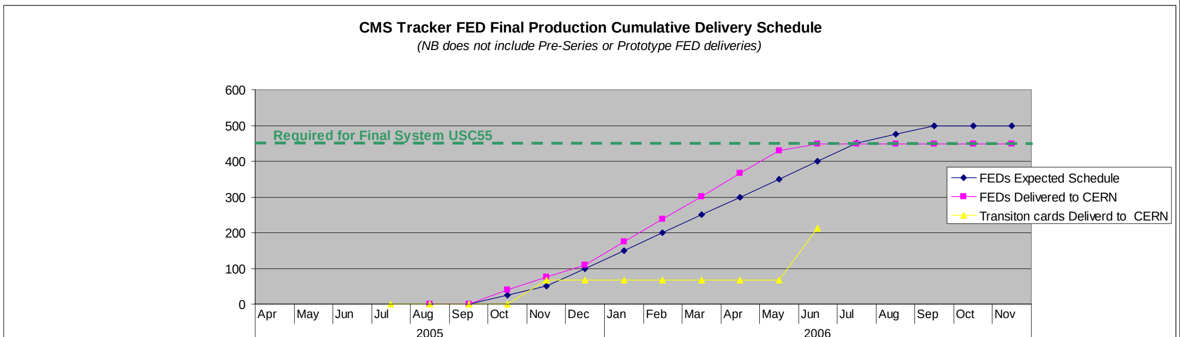
Project Monitor Form

Project: CMS FED **Date:** Wednesday 12 July-2006	**PMF number: 62** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Board Deliveries to CMS:
Total at CERN is now 448 FED boards.
This fulfils the requirements of the full Tracker readout system.
Remaining board deliveries are all spares.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
FEDs Expected Schedule					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
FEDs Delivered to CERN					0	0	40	75	110	174	238	302	366	430	448	448	448	448	448	448
Transiton cards Deliverd to CERN				0	0	0	0	68	68	68	68	68	68	68	212					

Production:

Final batch of ORx from CERN have been sent on to eXception for post fitting on last batch of FEDs.

The final 12 boards which will not have ORx fitted are already at RAL. Test with fake data?

Currently investigating another 12 boards at RAL with various faults.

The 4 faulty boards sent back from CERN have all been repaired and returned.
1 had faulty Temp chip (which caused spurious board shutdown)
3 had subtle problem with ACE controller. On these boards the ACE controller did not work if the supply voltage was greater ~ 3.2 V? This meant it would work in some VME crates but not others. Reason not understood. Replacing ACE fixed problem.

see details in Production spreadsheet.

SLINK Transition Card

Second and final manufacture batch of 430 cards delivered to RAL on schedule June 1st.
Of these 144 have passed tests using FEDKit and delivered to CERN.
About 3 cards have failed test.

CERN Integration :

FRL crate acceptance setup now being systematically run overnight on all FEDs at CERN.

System comprises of 2 Crates with 30 FEDs being readout out in merged mode to 15 FRLs with 2 FMM cards for throttle and TTCci + splitter for clocks.

Previous reported problems are now all understood and fixed.
FED hang ups in ZS mode were due to missing Fake triggers.
FED hang up during monitoring was due to side effect of reading certain FE registers during event readout. It was not noticed before as previously the monitoring rates were lower.
CRC errors in first run due to DAQ initialization.

Vertical Slice Tests
A major milestone has been achieved.
FEDs are now successfully routinely operating at target LHC event rates
FED in Fake Data mode and ZS Lite data format.
100 KHz random trigger rate and 3% occupancy
Nb FRL events are checked for CRC errors but not yet for event format consistency.

All FEDs previously installed in 186 are being exchanged with boards that have been put through FRL acceptance tests in 904.
Crates in186 are still awaiting connection to Tracker optical cables.

Firmware :

FE FPGA buffer depth on each channel was doubled from 2Kbytes to 4 Kbytes (adding second BRAM). This should increase event rates in Virgin Raw Data modes.

Software :

Gareth Rogers has returned as a CERN summer student.
One task is to integrate CF Firmware loading tool into final software.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Attend CERN Safety Training	Done		
Send TTCoc files to Jan Troska		IC	01-03-06
Implement SPY mode in Delay FPGA		ST	01-06-06
Implement additional status word in BE header		ST	01-06-06
Fix html files at eXception		JC	01-07-06
Add partial empty, half full flag register		ST	01-07-06

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Send TTCoc files to Jan Troska	IC	01-08-06
Implement SPY mode in Delay FPGA	ST	01-09-06
Implement additional status word in BE header	ST	01-09-06
Fix html files at eXception	JC	01-09-06
Add partial empty, half full flag register	ST	01-09-06

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** J. Coughlan **Date:** Wednesday 12 July-2006		**PMF number: 62** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05	01.05.06	
36	Last FED installed at USC55	26.07.06	31.09.06	
37	Power on Tracker	01.08.06	30.11.06	
38	Readout test with Tracker	01.10.06	01.02.06	
39	LHC test run	02.04.07	01.07.06	