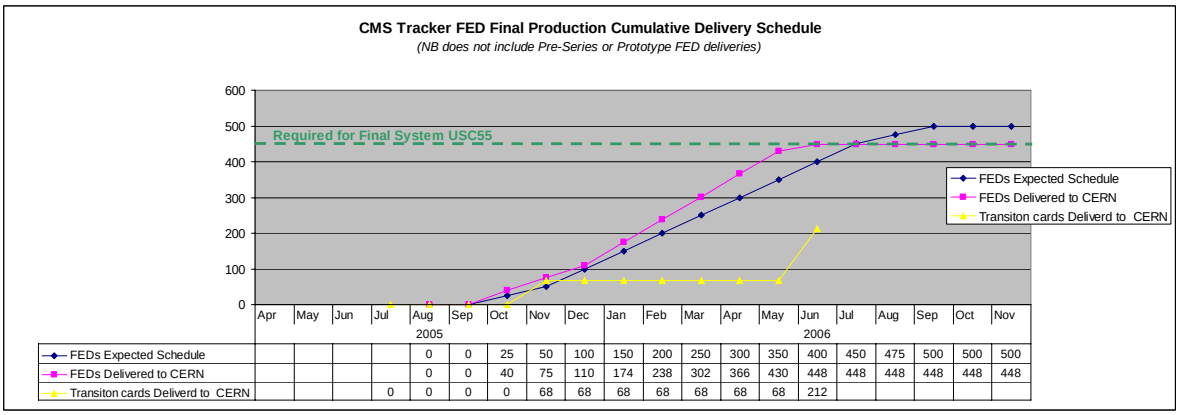
Project Monitor Form

Project: CMS FED **Date:** Wednesday 12 July-2006	**PMF number: 62** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

Board Deliveries to CMS:
Total at CERN is now 448 FED boards.
This fulfils the requirements of the full Tracker readout system.
Remaining board deliveries are all spares.



	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
FEDs Expected Schedule					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
FEDs Delivered to CERN					0	0	40	75	110	174	238	302	366	430	448	448	448	448	448	448
Transiton cards Deliverd to CERN				0	0	0	0	68	68	68	68	68	68	68	212					

Production:

Final batch of ORx from CERN have been sent on to eXception for post fitting on last batch of FEDs.

The final 12 boards which will not have ORx fitted are already at RAL. Test with fake data?

Currently investigating another 12 boards at RAL with various faults.

The 4 faulty boards sent back from CERN have all been repaired and returned.
1 had faulty Temp chip (which caused spurious board shutdown)
3 had subtle problem with ACE controller. On these boards the ACE controller did not work if the supply voltage was greater ~ 3.2 V? This meant it would work in some VME crates but not others. Reason not understood. Replacing ACE fixed problem.

see details in Production spreadsheet.

SLINK Transition Card

Second and final manufacture batch of 430 cards delivered to RAL on schedule June 1st.
Of these 144 have passed tests using FEDKit and delivered to CERN.
About 3 cards have failed test.

CERN Integration :

FRL crate acceptance setup now being systematically run overnight on all FEDs at CERN.

System comprises of 2 Crates with 30 FEDs being readout out in merged mode to 15 FRLs with 2 FMM cards for throttle and TTCci + splitter for clocks.

Previous reported problems are now all understood and fixed.
FED hang ups in ZS mode were due to missing Fake triggers.
FED hang up during monitoring was due to side effect of reading certain FE registers during event readout. It was not noticed before as previously the monitoring rates were lower.
CRC errors in first run due to DAQ initialization.

Vertical Slice Tests
A major milestone has been achieved.
FEDs are now successfully routinely operating at target LHC event rates
FED in Fake Data mode and ZS Lite data format.
100 KHz random trigger rate and 3% occupancy
Nb FRL events are checked for CRC errors but not yet for event format consistency.

All FEDs previously installed in 186 are being exchanged with boards that have been put through FRL acceptance tests in 904.
Crates in186 are still awaiting connection to Tracker optical cables.

Firmware :

FE FPGA buffer depth on each channel was doubled from 2Kbytes to 4 Kbytes (adding second BRAM). This should increase event rates in Virgin Raw Data modes.

Software :

Gareth Rogers has returned as a CERN summer student.
One task is to integrate CF Firmware loading tool into final software.