Project Monitor Form

Project: CMS FED **Date:** Friday 12-July-2002	**PMF number: 16** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

For details of design implementation and progress refer to minutes of FED design meetings of **June 12th**, **June 25th** and **July 5th** .

Schedule:

Reviewed schedule again with Designers & Drawing office.
Progress on BE schematics slower than anticipated. No single reason.
Finalising details of signals. More work on de-coupling scheme for FPGAs. Power circuit is more sophisticated.
More detailed week by week schedule has been produced taking into account details of vacations.
For milestone of 2 x assembled cards delivery to RAL it looks like we slip from end of September to **2rd week November**.
Largest uncertainty is time for layout & routing at board level (allowed 4 weeks Drawing Office).
New schedule released **v 1.3** (04.07.02).
Customer has accepted these changes.

Expenditure :
Electronic components on FK50800:
FY 2001/2002 = £ 8 K
FY 2002/2003 = £ 7 K

Manufacture:
Orders placed for majority of Power block components.

Design:

Front End Module:

Carried out final review of schematics and layout v 30.05.02.
Prior to final routing of complete module (already routed within 3 sub-modules)
List of (minor) modifications compiled.
Majority of changes relate to improvements in de-coupling of FPGAs.

CERN have reported problems with latest Opto Rx ASIC settling time.
2 options allowed for : Extra control lines / Peaking capacitor on output in parallel with load Resistor.

Had discussions with Bergquist rep on thermal dissipation from OptoRx.
Thermal pads under OptoRx don't seem suitable due to difficulty in assuring thickness. If

needed a better choice might be liquid. Have to discuss with assembly company in any case.

FE Module now "on hold". But in good shape.
Implement mods and route within next 4 weeks.

BE Module :

BE FPGA (2000) + QDR SRAMs + TTCrx + PIN DIODE + BUFFERS + J2 + J0 (SLINK/TTS/VME)

Schematics released v04.07.02
Differential PIN DIODE recommended by Bruce Taylor. Go with fibre lead from Front Panel connector to TTC at back end. Still to include TTC PIN DIODE circuit. (Nb we will keep option to use either differential or single-ended PIN diode.).
TTS is brought to both J2 and J0

VME FPGA (1000) + SYSTEM ACE + CONFIG EPROM + SER EPROM + BUFFERS + JTAG + J1 (VME)

Schematics expected by end of next week.
Simplified FPGA configuration scheme. No need for second FLASH memory device.
Simplified JTAG test/load chain.
Expect schematics back from Drawing Office for inspection by middle of week after next.

POWER : PS SUPERVISOR + HOT SWAP CONTROLLERS + DC-DC CONVERTERS + LINEAR REGULATOR + VOLTAGE MONITOR + RESET GENERATOR

Documentation describing design released.
Lots of features: Power from standard VME64x supplies.
Hot swap sequencing, protection against Over Voltage, Under Voltage, Over Current, Over temp, Voltage monitoring.
Internal review of design schematics (v 04.07.02) completed.
List of mods compiled and implemented in v 11.07.02.

Firmware:

FE FPGA firmware is being updated.
Auto Cal logic removed, controls for OptoRx, Temp Sensor, DAC added. header finding logic simplified.
Will fit in 1500 part. 40 MHz clock logic meets timing. 80 MHz clock logic is close to meeting timing.
Power consumption measurements in progress.

DAQ issues:

At Readout Unit Working Group meeting at CERN (11.06.02) a proposal for use of VME64x features for plug & play board addressing was accepted.

CERN DAQ group are suggesting FED users could adopt Compact PCI as used in data merging

crates. VME64x fulfils our requirements in terms of mechanics, speed, power and user i/o. Compact PCI may also satisfy our needs, but we estimate switching standards could add between 3 and 6 months to production schedule which is not acceptable to the customer.

Actions from the previous PMF

Action	Status	Who	Target date
Revise power/current tables for FE FPGA in VirtexII model.	In progress	ST/WG	31-07-02
Route FE sub-modules. Rats nest FE Module.	Done	CD	
Component ordering list from FE Module.	Done	CD	
Organise FE Module final review.	Done	CD	
Pin out BE and VME FPGA blocks.	BE done. VME in progress	ST	14.06.02
Produce BE and VME FPGA block schematics rats nest.	BE done. VME in progress	CD	21.06.02
Produce Power block design.	Done	JS	
Produce Power block schematic rats nest.	Done	CD	
Produce BE module layout.	In progress	RH	28.06.02
Incorporate latest modifications to FE FPGA firmware.	In progress	WG	08.07.02
Verify size, speed and power of FE-FPGA design.	In progress	WG/ST	08.07.02
Verify component procurements for 2 boards.	Done	JC	

Actions outstanding and new actions

Action	Who	Target Date
Pin out BE and VME FPGA blocks.	ST	12-07-02
Produce BE and VME FPGA block schematics rats nest.	CD	17-07-02
Produce BE module layout (on paper).	RH	31-07-02
Incorporate latest modifications to FE FPGA firmware.	WG	31-07-02
Verify size, speed and power of FE-FPGA design.	WG/ST	31-07-02
Verify component procurements for 2 boards.	JC	21-06-02
Complete schematics BE module.	CD	19-07-02
Hold review BE module.	JC	26-07-02
Implement FE module final changes.	CD	02.08.02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 16**		
Project Manager: R. Halsall **Date:** Friday 12-July-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02		21-03-02
5	FE Module Feasibility Review	28-02-02		08-05-02
7	**Board Level Feasibility Review**	**25-02-02**		**25-02-02**
8	Delay FPGA Interim Review	11-03-02		27-03-02
9	Front End FPGA Interim Review	28-02-02	31-07-02	
10	Back End FPGA Interim Review	04-03-02	30-08-02	
11	FE Module Final Review	18-06-02		25.06.02
12	BE Module Interim Review	28-06-02	26.07.02	
13	Schematics finalised	05.08.02		
14	Layout & Routing done	16.09.02		
15	Full Board Design Final Review	23-09-02		
16	**IDR Customer Production sign off**	**07-10-02**		
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11-11-02**		
18	OptoRx for Batch 0 at RAL	26-08-02		
19	Batch 0 review	11-04-03		
20	OptoRx for Batch 1 at RAL	01.04.02		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04-07-03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04-12-03**		