Project Monitor Form

Project: CMS FED	**PMF number: 39**
Date: Tuesday 11 November-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

PMC test bench is being set up again to complete delivery of remaining cards.
Due to work on last batch of FEDs Ivan has not been able to start on PMCs.
Jonathan Godwin is now expected back in December and could take up repair work then.

FEDv1:

Manufacture

Status of last 6 boards (immersion tin):
06. Basically working, problems under two of the delay BGAs that require looking at.
07. Basically working, problem with a open circuit under the TTC BGA on CLK40DS1.
08. Bad. Two of the FE FPGAs had to be bypassed to get connectivity with the chain, after which a host of other errors were discovered with other interconnects.
09. FPGAs removed by Saetech but the short remains present. The card is still at Saetech.
10. Bad. Three of the FE FPGAs had to be bypassed to get connectivity with the chain, one or two errors show up on the remaining nets tested.
11. Unknown, board still at Saetech.

01 At IC
02 At RAL
03: At RAL Modified for 1Vpp ADC. TTCrx needs Bscan check.
04: With Calice group at RAL.
05 At CERN. Modified for 1Vpp ADC.

Re-balling of large FPGAs going ahead (cost is £35 each).

CALICE 2 pcbs received. PCB company DDI. Same immersion tin finish. Both look good.

Delivery:
First FED nr 005 was shipped to CERN on Nov 3rd. Peaking caps all removed. Modified for 1Vpp ADC operation using 100 Ohm across ADC inputs. Strengthening bar added. TTCrx fibre added. All channels tested at RAL before delivery.
Delivered Firmware: Delay 02_17; FE 03_09; BE 02_28; VME 11_00 (20)
Results from initial system tests at CERN look good.

System Tests

3 LHC crates delivered to RAL on Nov 3rd.
PS tested.
Crate powered on with up to 6 FEDs.
Note Fan tray does not extend under Transition slots?

Mechanics for insertion with VME64x handles doesn't look very rigid.
Get 6U slot kit and install 2nd set of SBS cards in crate. Needs another PC.
Use this crate for system software tests.

S-LINK readout. Firmware nearly implemented. Transition card needs minor modifications.
Ready to begin tests with FEDKit next week.

TTC cards sprang into life at same time OptoTester was brought to RAL because -12V was only connected to test crate then!

Firmware

Updated documentation and zipped source files for all designs on FED-UK web page.

Delay-FPGA:

Documentation was updated by Ed before final handover of design to Saeed.
To do: Test Spy Channel. Minor changes needed in VME serial for this.

FE-FPGA:

In process of understanding pedestal memory loading in order to start tests of zero suppression logic.
Proposal from Emlyn for increasing FE buffer depths.

BE FPGA:

S-LINK logic is almost ready to test.

VME FPGA:

Documentation was updated by Ed before final handover of design to Saeed.
To do: System ACE interface and EPROM interface under preliminary study.
Mods for testing spy channel needed. Clock resetting could be improved.