Project Monitor Form

Project: CMS FED **Date:** Wednesday 11-June-2003	**PMF number: 32** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Corrected Front Panels have not yet been delivered (were expected last week.) Bob T. is on leave. Almost 30 PMCs are otherwise ready to ship.
Remaining cards will be put on hold (unless there is a strong demand from CMS) in order to focus effort on FEDv1.

The list showing location and status list of "old" PMCs has been updated.

FEDv1:

Manufacture

3 boards (incl 1 with 8xOptoRx) now expected back by Friday 20th June.

Assembly company have installed new machines. Should ensure faster turnarounds in future. Requires an updated format for data files from Drawing Office (being done.)

Assembly company spent some time investigating problems reported on Atlas 9U boards. Traced to PCB manufacture process (also Express Circuits.) These effects were not observed on FEDs.

Firmware

Progress has picked up again.

Delay-FPGA:
Minor bug fixes from Matt have been incorporated. Clock skewing appears to be working now.

FE-FPGA:
In Scope mode we can now see correct header & data output from all 12 fibres. (order of output of channels is reversed from expected?)
Now implementing basic test of Header Finding logic by feeding back "ticks and header bits" pattern data from BE via Test card.
DAC offset control tested, observe expected shifts in pedestals.

BE FPGA:
Functional simulation works up to VME-Link output. Recent effort has gone into meeting the post layout timing constraints, especially for QDR I/O. Bug found in Xilinx DCM functional simulation caused some confusion. Design is now just about to be tested on FED.

VME FPGA:
After considerable effort the serial read-back of FE registers is now fully working.

Design of VME-Link receiver is in progress (missing link in readout chain.) S/W readout registers agreed. Transfer speed to buffer memory verified.

Others
Distribution for clocks and reset logic “was rationalised” for all FPGAs in chain.
A possible work around (tying down design with Relational Macros before adding ChipScope) to permit reliable use of Chip-Scope in our designs is being tried out.
Rob has fitted Xilinx reference design for “Channel Link” on development board.

Software
Matthew P. is testing FED Configuration class commands.
Fed API. Scheme for FEDVME class is ready for discussion.