Project Monitor Form

Project: CMS FED **Date:** Wednesday 11-June-2003	**PMF number: 32** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Corrected Front Panels have not yet been delivered (were expected last week.) Bob T. is on leave. Almost 30 PMCs are otherwise ready to ship.
Remaining cards will be put on hold (unless there is a strong demand from CMS) in order to focus effort on FEDv1.

The list showing location and status list of "old" PMCs has been updated.

FEDv1:

Manufacture

3 boards (incl 1 with 8xOptoRx) now expected back by Friday 20th June.

Assembly company have installed new machines. Should ensure faster turnarounds in future. Requires an updated format for data files from Drawing Office (being done.)

Assembly company spent some time investigating problems reported on Atlas 9U boards. Traced to PCB manufacture process (also Express Circuits.) These effects were not observed on FEDs.

Firmware

Progress has picked up again.

Delay-FPGA:
Minor bug fixes from Matt have been incorporated. Clock skewing appears to be working now.

FE-FPGA:
In Scope mode we can now see correct header & data output from all 12 fibres. (order of output of channels is reversed from expected?)
Now implementing basic test of Header Finding logic by feeding back "ticks and header bits" pattern data from BE via Test card.
DAC offset control tested, observe expected shifts in pedestals.

BE FPGA:
Functional simulation works up to VME-Link output. Recent effort has gone into meeting the post layout timing constraints, especially for QDR I/O. Bug found in Xilinx DCM functional simulation caused some confusion. Design is now just about to be tested on FED.

VME FPGA:
After considerable effort the serial read-back of FE registers is now fully working.

Design of VME-Link receiver is in progress (missing link in readout chain.) S/W readout registers agreed. Transfer speed to buffer memory verified.

Others
Distribution for clocks and reset logic “was rationalised” for all FPGAs in chain.
A possible work around (tying down design with Relational Macros before adding ChipScope) to permit reliable use of Chip-Scope in our designs is being tried out.
Rob has fitted Xilinx reference design for “Channel Link” on development board.

Software
Matthew P. is testing FED Configuration class commands.
Fed API. Scheme for FEDVME class is ready for discussion.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Produce FED software driver lib API.	Basic scheme done. IRT to continue.	JC	
Test read-back of FE.	Done	EF/JC	
Test FE to BE FPGA and QDR data write path.		IC/ST	04-04-03
Send first batch of FED-PMCs to CERN.		JG/JC	09-05-03

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test FE to BE FPGA and QDR data write path.	IC/ST	13-06-03
Send first batch of FED-PMCs to CERN.	JG/JC	27-06-03
Loop back test on FED with apv headers from BE.	IC	23-06-03
Start test on FED of VME-Link receiver.	EF	23-06-03

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 32**		
Project Manager: J. Coughlan **Date:** Thursday 29-May-2003		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.3**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	**Project Spec sign off**	**21.12.01**		**05.02.02**
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	**Board Level Feasibility Review**	**25.02.02**		**25.02.02**
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	**IDR Customer Production sign off &PCB Tape Out**	**07.10.02**		**06.12.02**
17	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**11.11.02**		**22.01.03**
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	**Batch 1 (10 off) Assembled boards at RAL**	**04.07.03**		
22	Delivery Batch 1 to CERN start	12.09.03		
23	**Delivery Batch 1 to CERN completed.**	**04.12.03**		