

## Project Monitor Form

<b>Project:</b> CMS FED <b>Date:</b> Thursday 11 May-2006	<b>PMF number:</b> 61 <b>Sheet:</b> 1 of 2
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Project Implementation phase.

  

### FED Production

Board Deliveries to CMS: Remains on schedule.  
 Total at CERN is now 366 boards.

  

**CMS Tracker FED Final Production Cumulative Delivery Schedule**  
*(NB does not include Pre-Series or Prototype FED deliveries)*

	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov
Planned at CERN					0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
Actual at CERN					0	0	40	75	110	174	238	302	366	366	366	366	366	366	366	366

**Production:**

Manufacture continuing to plan. Expect final assembly run of 35 boards in May.  
 Notified of shortage of free issue 10 nF capacitor very late. Stock had to be ordered from Japan by eX.

Several boards have exhibited spurious failures during the JTAG Boundary Scan test.  
 Following investigation suspect incorrect termination of the JTAG TCK and TMS lines coming out of the XCACE device U111. The affected boards can be modified to allow test to be carried out.

The unused FEDv1 prototypes have been sent to eXception for ORx recovery, along with ORx already removed and a few unused spares. Total 96 pieces.

We have verified that all (non ORx specific) assembly test procedures can be carried out on any remaining boards without ORx (should be < 10 boards).

RAL Testing status also on schedule, see Production [spreadsheet](#).

  

### SLINK Transition Card

Order of remaining 430 Transition cards are still due for delivery by end of May.

  

### CERN Integration :

During Tracker week Ivan assisted Oz in moving crates of FEDs from B904 to B186 for Tracker

integration (latter is now 9 crates x 16 FEDs).

Ivan also installed J0 JTAG backplane cards with rear front panels for VME boot device programming in B186. All VME EPROMs in these crates can now be programmed in situ using this system.

Vertical slice tests phase 2 Throttle Loop :

Full crate system with FRL merged readout and FMM throttling has been demonstrated to be working at modest trigger rates.

Now investigating overflow occurrences, diagnostics and system recovery in more extreme data taking conditions...

Test conditions:

Single board tests with FED in FAKE data mode various occs. Throttle direct to APVe (note FMM removed from loop to simplify test). Triggers at fixed intervals, various rates from LTC. Readout via FRL. FED BE logic is set up to freeze when Out of Sync occurs in order to inspect the buffer status at overflow.

Scope mode :

Appears to run ok with throttling active. Q. Do L1A and Frame counters match at run ends?

Virgin Raw data :

At high (multi kHz) rates FED FE buffer overflows generates OOS. As expected since FE buffer only holds up to 3 events. One solution is to double buffer depth (requires 12 more BRAMs). Another to change the logic for over flow flag in Raw Data mode to use a Frame header counter.

ZS Data :

Appears to run ok until the FED throttle is asserted then immediately hangs.

E.g. Fails with 100kHz ; 3% occ. (\*)

Ok at 50kHz ; 3% occ.

Need remote access to diagnostics at B904.

(\*) running with FED Tester with comparable conditions at RAL without problem.

Further tests show that the FED is actually stuck in WARN state (not OOS). Appears to be a deadlock with LTC stopping triggers in WARN and FED BE waiting for FE to supply missing frames. See dump below

## BE Control Registers:

```

1)  Trigger Source = $ 1
2)    BE Mode = $ b
3)    TTCrx Ctrl = $ 6d3
4)    Test Register = $ 0
5)    FE Enable = $ ff
6)    BE Link = $ 1
7)    BE Enable = $ 0
10)   FED ID Reg = $ 2
13)   DAQ Register = $ 0
14)   Trk Header = $ 1
30) Default Evt Type = $ 1
31)   FOV = $ 0
15)   BX offset = $ 1 ; 1
33)   Bx Max = $ dec ; 3564

```

## BE Status Registers:

```

21)   FPGA Usercode = $ 22000377
17)   L1A ctr = 9055
18)   BX ctr = 1848 $738(hex)
23)   Total Frame ctr = 8927
19)   Unread Frame ctr = 0
22)   Unread Word (64bit) ctr = 0 $ 0
20)   TTC Ready = $ 1
27)   TTC ChanB Short Brcdcast : Data = $ 0
26)   TTC ChanB Long Single : TTC Addr = $0000 ; Sub Addr = $00 ; Data = $00
29)   TTS Status & BX at New Orbit:
      TTS bits = $1 ; TTS status = WARNING OVERFLOW
      Bx Ctr Value at New Orbit = $dec (3564)
16)   BE Status = $ 6f0000e0

```

Bit :	Condition	Status	Bit :	Condition	Status
31 :		0	15 :		0
30 :	FE FPGA Data Fifo EMPTY	1	14 :	FE FPGA Data Fifo FULL	0
29 :	FE Evt Length Fifo EMPTY	1	13 :	FE Evt Length Fifo FULL	0
28 :	L1A & BX Fifo EMPTY	0	12 :	L1A & BX Fifo FULL	0
27 :	Trk Hdr Fifo EMPTY	1	11 :	Trk Hdr Fifo FULL	0
26 :	Tot Length Fifo EMPTY	1	10 :	Tot Length Fifo FULL	0
25 :	Frame Addr Fifo EMPTY	1	9 :	Frame Addr Fifo FULL	0
24 :	QDR EMPTY	1	8 :	QDR FULL	0
23 :		0	7 :	Tracker Header Monitor READY	1
22 :	FE FPGA Data Fifo PARTIAL FULL	0	6 :	TTCrx READY	1
21 :	FE Evt Length Fifo PARTIAL FULL	0	5 :	BX Error at Orbit Reset	1
20 :	L1A & BX Fifo PARTIAL FULL	0	4 :	BackPressure Flag	0
19 :	Trk Hdr Fifo PARTIAL FULL	0	3 :	SLINK FULL Flag	0
18 :	Tot Length Fifo PARTIAL FULL	0	2 :	SLINK DOWN	0
17 :	Frame Addr Fifo PARTIAL FULL	0	1 :	Internal Freeze	0
16 :	QDR PARTIAL FULL	0	0 :	Temperature Interrupt b	0

```

34) FMM Test Register: Ready/Busy/Out of Sync/Warn Overflow = $0
   0 / 0 / 0 / 0 /

```

## TTC RESYNC

Some initial problems caused by non enabling of TTCrx chan B receiver.

On receipt of resync BE buffers were reset but not FE buffers. FE was modified to correct this. BE also had a small mod to handle this.

This was done and is now tested at RAL and CERN.

A wait of 21 micro secs in BE between receipt of Resync and assertion of Ready is implemented. This was according to the FED specifications provided by Matt Pearson in the TTC requirements doc. The reason was to allow time for APV pipelines to be emptied.

This delay is no longer specified by the Trigger Control system rules and should be removed for final system. This implies that on receipt of a resync the FED would reset all internal buffers immediately and any pending data in the FED will be lost.

Question to CERN: In VME readout mode should the VME buffers also be reset by TTC resync command for final system compatability?

## Other issues:

Software dump of registers during data taking is also causing the FED to "fall over"?

Oz has observed intermittent FPGA loading problems on some FEDs from 5<sup>th</sup> batch to CERN. Ivan is investigating timing sequence during FPGA startup. Could be sensitive on crate power sequencing?

**Actions:**

Obtain remote access from RAL to test system to investigate FED status at OOS.  
Arrange with CERN for RAL engineer visits to assist diagnosis and correction.

**Firmware :**

BE FPGA test register which was used for generating Throttle signals, to validate FED-FMM connectivity, had side effect of skewing +/- differential TTS outputs.

As test register is now removed it should be possible to remove APVe deglitch logic which was added to cope with skewing.

Following release of latest VME ...32B some random data corruption was seen at CERN in legacy systems using electrical SBS connections. The problem is not seen with CAEN or SBS optical systems either at RAL or CERN. If legacy systems cannot be upgraded they must revert to previous VME ...322.