Project Monitor Form

Project: CMS FED **Date:** Monday 11-February-2002	**PMF number: 08** **Sheet:** 1 **of** 2

News and comment
Feasibility Study continues.

Procurement:
Bob has placed order for 500 ADCs.
We will also order 1000 ADC driver AD8138 for 10 cards.
As it still does not seem possible to get an order for FE FPGA (3M) parts through this FY we will wait. In any case we need to clarify situation with regard to Xilinx franchises and quotes.

Front End Module:
Chris showed a zeroth order layout showing space taken by currently known components on FE module.
He has sketched out the block level layout of board, keeping in mind the aim of a modular design.
He has distributed a paper schematic of a module containing 2 analogue channels. This needs to be reviewed by James and Adam.
Chris will then produce a first order layout of components up to ADCs on FE Module without tracking.

CERN (Francois Vasey et al) are about to fix OptoRx pin arrangement with NGK.
Adam will produce his recommendations for the pinout.

James has verified performance of VREF components on test board.
He has also reviewed temperature/voltage monitoring devices and has identified a possible candidate ADM1022.
He is continuing design of filter for OptoRx power supplies.

Firmware:
Delay chip:
Due to restrictions on the use of clock signals to BUFGMUXes the original proposal for selecting between 4 clock phases on output of DCM is not possible for all 4 DCM channels. Ed is actively investigating alternative strategies (eg removing data buffering functionality from design) However it should be acknowledged that the design is working at the limits of the resources of 40K part. The next step in DCM resources is the 200K part.

Board level:
Saeed is continuing work on the board overviews.
His first priority is identifying power supply requirements of components. He is attempting to use Xilinx power estimation tools to obtain consumption of Bill's FE FPGA design.
It is believed the board requires following supplies: +1.5V, +3.0V, +/- 5V, although there is some debate on whether +3.3 V is also necessary.
The aim is to avoid on board regulators if possible.
In parallel Saeed is investigating the JTAG , FPGA configuration and the clock distribution chains.

Other issues:
Rob has asked Paul Hardy and Mark Willoughby to look into CADENCE tool's ability to import Xilinx FPGA symbols.

Actions from the previous PMF

Action	Status	Who	Target date
Pass component details for purchases this FY to Bob T.	Done	JC	
Investigate tools to create CADENCE symbols of Xilinx FPGA.	Done. Request to Paul Hardy.	RH	
Test key aspects of Delay FPGA on development board in Lab	In progress	EF/RH	31-02-02
Produce preliminary pinout of Delay FPGA.	In progress	EF	11-02-02
Obtain estimate for PCB manufacture 500 H1FTT as guide of CMS costs.	On going	CD	18-02-02
Specify board level voltage and current requirements.	In progress	ST	18-02-02
Ask R. Stephenson if we can borrow simulations tools license for James's PC.	On going	RH	11-02-02
Investigate temperature monitoring of FE Module (OptoRx/Virtex)	Done	JS	
Produce proposal for web pages reorganisation	On going	AB	04-02-02

Actions outstanding and new actions

Action	Who	Target Date
Test key aspects of Delay FPGA on development board in Lab	EF/RH	31-02-02
Produce preliminary pinout of Delay FPGA.	EF	31-02-02
Obtain estimate for PCB manufacture 500 H1FTT as guide of CMS costs.	CD	18-02-02
Specify board level voltage and current requirements.	ST	18-02-02
Ask R. Stephenson if we can borrow simulations tools license for James's PC.	RH	31-02-02
Specify board level voltage and current requirements.	ST	18-02-02
Pass ADC driver component details for purchase this FY to Bob.	JC	18-02-02
Produce recommendations for OptoRx pin out	AB	18-02-02

Check Chris's schematic.	JS/AB	18-02-02
Produce 1st order FE module analogue component layout.	CD	18-02-02

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 08**		
Project Manager: R. Halsall **Date:** Monday 11-February-2002		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01		05-02-02
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	