

Project Monitor Form

Project: CMS FED Date: Monday 10-December-2001	PMF number: Sheet: 1 of 2
<p>News and comment</p> <p>Feasibility Study continues</p> <p>Chris has commenced work on the Front End Module overview now that Generic ADC Front End is out. Initial plan is to get components into library and look at module size.</p> <p>We have been told by the customer that NGK has been selected as Opto Receiver – however no contract has been signed yet.</p> <p>James is progressing with simulation tools. Tools now run and he is working his way through the open book manuals. We will need to attach simulation models to components as we wish to use same schematic for simulation as PCB design.</p> <p>Ed has made progress with Delay FPGA – design has been fitted and simulated both functional & back annotated timing. Functional simulation in combination with the FE FPGA within Bill Gannon’s test bench.</p> <p>We have received</p>	

Actions from the previous PMF			
Action	Status	Who	Target date
Develop draft Project Spec	In Progress	JAC	xx-01-02
Develop draft schedule	In Progress	JAC	xx-01-02

Actions outstanding and new actions		
Action	Who	Target Date
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	RH	17-12-01
Organise a Board Level Design Meeting	RH	20-12-01
Organise hand over meeting for Back End FPGA	RH	19-12-01
Pass schematic for Analogue part of Front End module to DO	JS/CD	17-12-01
Test key aspect of Delay FPGA on development board in Lab	Ed/All	31-01-02

Project Monitor Form- milestones

Project:		PMF number:		
Project Manager:		Sheet: 1 of 2		
Date:				
	Milestones from Project Management Plan Version:	date due in PMP	predicted date	date done
1	User Requirements Document			xx-yy-01
2	Project Spec sign off	Pre-PMP	xx-01-02	
3	Complete Delay Line FPGA Feasibility Study	Pre-PMP	xx-01-02	
4	Complete Front End FPGA Feasibility Study	Pre-PMP	xx-01-02	
5	Complete Back End FPGA Feasibility Study	Pre-PMP	xx-01-02	
7	Complete VME FPGA Ancillary Feasibility Study	Pre-PMP	xx-01-02	
8	Complete Ancillary Circuits Feasibility Study	Pre-PMP	xx-01-02	
9	Complete Board Level Feasibility Study	Pre-PMP	xx-01-02	