

Project Monitor Form

Project: CMS FED Date: Monday 10-June-2002	PMF number: 15 Sheet: 1 of 2
<p>Project Implementation phase.</p> <p>News and comment</p> <p>Refer for details of design progress to minutes of FED design meetings of May 8th, May 17th and May 29th.</p> <p>Updated project schedule v1.2 was released on May 10th. Manufacture date for first 2 full scale prototypes moved back approx 8 weeks. Expect assembled cards back at RAL mid September. Customer has approved this schedule change.</p> <p>Staff effort used in FY 2001/02 on CMS FED project codes [FK50030/FK50040/FK50050] was 4.87 SY (c.f. with projected value of 5.60 SY) in line with expectations.</p> <p>IDR 002 of FE Module design was held at May 8th design meeting.</p> <p>FED analogue design presented by James at customer meeting of May 10th.</p> <p><i>Manufacture:</i> Orders placed for connectors, QDR SRAM, and remaining configuration devices. TTCrx PIN diodes ordered. Remaining items to order are Power block components.</p> <p><i>Front End Module:</i></p> <p>Schematics and layout have been produced. 3 sub-modules: ADC, OptoRx, FE-FPGA ADC sub-module has been routed. OptoRx power filter has been completed. Spikes observed due to APV header levels have been suppressed by damping resistors. Layout confirms that 96 channels will fit on 9U board.</p> <p>Analogue design (single stage Elantec) was examined at CERN and approved by Francois. Heat dissipation schemes still under investigation, but not considered to be major concern. More detailed models of de-coupling of OptoRx were supplied by Francois.</p> <p>Next step to route OptoRx and FE-FPGA modules. Bring up sub-modules to FE Module level at rats nest. Further review before routing FE Module.</p> <p><i>Back-End Module:</i> 3 blocks identified: BE-FPGA, VME-FPGA, Power. Components for first 2 blocks entered in schematics.</p>	

Pin out for BE-FPGA done.

S-LINK signals taken to P2 (option to group data in LVDS pairs if necessary.)

Pair of QDR SRAM solution adopted (i.e. half speed) using 2-word burst chips.

Pin out for VME-FPGA in progress.

Opted to remove second Compact Flash configuration device.

VME buffers supporting hot swap selected.

Power block design version 1 produced.

JTAG chain scheme updated:

2 chains for test (FE modules/BE module). Switch via jumpers to 1 chain (containing only Xilinx devices) for configuration. Remove VME JTAG registers (replaced by MPU/System ACE interface.)

TTCrx PIN diode and ASIC will be located on BE module connected by flying optical lead to Front Panel connector.

Firmware:

FE FPGA:

Updated list of modifications for FE FPGA firmware.

Major changes: remove Auto Cal logic; add controls for OptoRx, Temp Sensor, DAC; simplify header finding logic; refit for size and speed; measure power consumption using latest tools.

Software:

FED online software to be discussed at RUWG on June 11th at CERN.

Actions from the previous PMF			
Action	Status	Who	Target date
Produce 1 st order FE module analogue component layout.	Done.	CD/JS	
Update FE module analogue layout with Elantec opamp.	Done	CD	
Repeat measurements a la AD devices with Elantec opamp circuit on test board.	Done	JS	
Repeat simulations a la AD devices with Elantec opamp model.	Done	JS	
Revise power/current tables for FE FPGA in VirtexII model.	In progress	ST/WG	28-06-02
Revise FED schedule.	Done.	JC/RH	
Organise FE Module review.	Done.	JC	

Actions outstanding and new actions		
Action	Who	Target Date
Route FE sub-modules. Rats nest FE Module.	CD	14-06-02
Component ordering list from FE Module.	CD	14-06-02
Organise FE Module final review.	JC	21-06-02
Pin out BE and VME FPGA blocks.	ST	14-06-02
Produce BE and VME FPGA block schematics rats nest.	CD	21-06-02
Produce Power block design.	JS	11-06-02
Produce Power block schematic rats nest.	CD	21-06-02
Produce BE module layout.	CD	28-06-02
Incorporate latest modifications to FE FPGA firmware.	BG	08-07-02
Verify size, speed and power of FE-FPGA design.	BG/ST	08-07-02
Verify component procurements for 2 boards.	JC	21-06-02

Project Monitor Form- milestones

Project: CMS FED		PMF number: 15		
Project Manager: R. Halsall		Sheet: 2 of 2		
Date: Tuesday 30-April-2002				
	Milestones from Project Management Plan Version:1.2	date due in PMP	predicted date	date done
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01		05-02-02
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02		21-03-02
5	FE Module Feasibility Review	28-02-02		08-05-02
7	Board Level Feasibility Review	04-03-02	18-06-02	
8	Delay FPGA Interim Review	11-03-02		27-03-02
9	Front End FPGA Interim Review	28-02-02	12-07-02	
10	Back End FPGA Interim Review	04-03-02	30-08-02	
11	FE Module Final Review	18-06-02		
12	BE Module Interim Review	28-06-02		
13	Full Board Design Final Review	17-07-02		
14	IDR Customer Production sign off	31-07-02		
15	Batch 0 (2 off) Non- Opto Assembled boards at RAL	12-09-02		
16	OptoRx for Batch 0 at RAL	26-08-02		
17	Batch 0 review	13-02-03		
18	Batch 1 (8 off) Assembled boards at RAL	08-05-03		
19	Delivery Batch 1 to CERN completed.	12-09-03		
20				
21				
22				