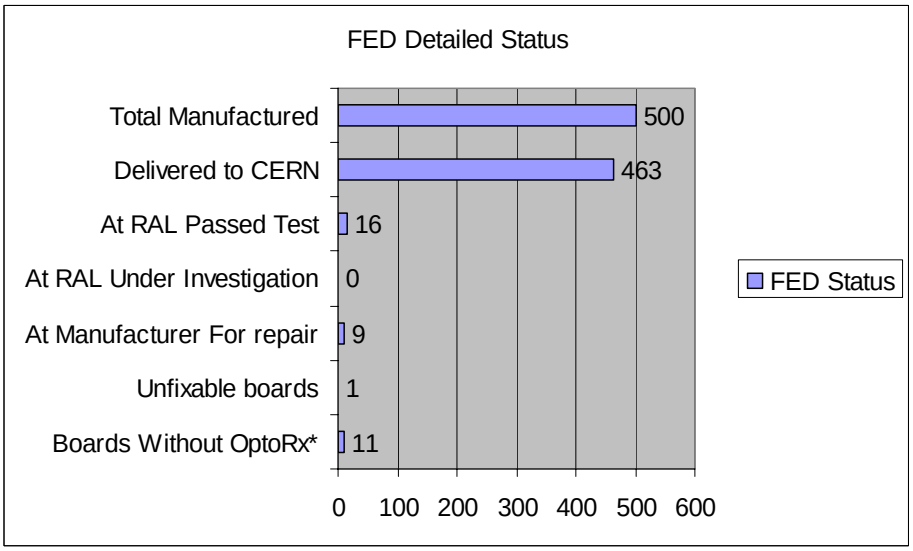
Project Monitor Form

Project: CMS FED	**PMF number: 65**
Date: Wednesday 10 January-2007	**Sheet:** 1 **of** 2

Project Implementation phase.

FED Production



Current good board yield = 98.0 %
Full details in Production spreadsheet.

FEDs

Delivery to CERN of the penultimate batch of 16 FEDs is delayed owing to a failure of the RAL crate cooling unit before Christmas. This should be repaired in January. These boards just require the full crate test.

Investigations have been completed and repairs identified on the last remaining 10 boards. All are now in for repair with manufacturer.
Will request to recover ORx from unfixable boards (1 so far) to put on unpopulated boards.

CERN USC Installation and Commissioning :

Cooling systems in USC are ready now. One full rack of FEDs with Transition cards (44) has been installed. Rack has been powered successfully but no readout tests yet. The DAQ group will be ready to start tests to FRL and FMM from February onwards. Plan is to install software and do readout tests with one rack before installing further crates.

Also need to implement any changes to Transition card FMM shielding beforehand (see below). As DAQ responsibles are recommending implementing shielding. Oz, Ivan and Saeed will propose convenient mechanical scheme on Transition card to connect connector to front panel. This could be then be done before February tests. The 44 Transition cards are all old cards with unshielded RJ45.

An updated installation schedule has also been released by Karl.

A FED Power Suppy in USC has already failed. Another one in B186 has also failed. Same failure mode as previously seen by us (and other CMS and ATLAS groups). More worryingly a repaired PS has also subsequently failed. Paul Harwood is informed.

SLINK Transition Cards

CERN Deliveries already completed.

A meeting has been held at CERN to discuss noise problems observed on links between APVe and FMM. These are caused by such various events as fluorescent lighting switching and have the bad effect of generating spurious Out Of Sync signals which hang the readout system. It is currently believed to be curable by improving grounding scheme between crates to avoid mains ground pickup.

Situation on FED/Transition cards summarized…

Noise effects have NOT shown up (yet) in tests of the FED/Transition crate to FMM crate links. However as the Transition card does use the same cables and connectors as the links between the APVE and the FMM crate we need to be aware if there are problems there.

We built first 70 Transition cards July 05 following existing DAQ specs of course. The RJ45 connectors on the FMM links did not have metal shields.

Some time later (Nov 05) we heard reported (unexplained) FMM link noise effects following the DAQ groups own lab tests and they suggested alternative grounding schemes and connectors.

As an insurance we fitted metal shielded connectors on the remaining batch of 430 Transition cards ser nr 71+. However, as we didn't want to change the card layout it means that in order to actually ground the connector a small link needs to be added between connector and existing nearby ground point (or front panel?) on card. We took the pragmatic approach not to fit such links until it was demonstrated they are needed (and didn't introduce other problems?).
If it's necessary this should be a simple (if tedious) job to do at least before we populate USC55.

Similarly we didn't retro fit shielded connectors on the first 70 cards already at CERN (apart from one I think as a test). But again it could be done (we have extra shielded connectors).

Software

Timing tests at RAL.

Firmware and System Integration Tests

The problem detailed in last report of complete stoppage of event readout in CERN FRL test system was resolved after visit by Saeed to CERN and discussions with DAQ group. The root cause was a misunderstanding of the handling of the SLINK reset signal. The protocol adopted by the DAQ group is slightly different from the published standard. The FED firmware had been changed to try and resolve the missing buffers effect seen in the Magnet tests.
A new BE firmware was released to cure all FRL problems. Event readout is working, but we are still waiting for results from TOB tests to see if missing buffers are also cured.

Update on the other modifications..

```
1. Swap FE Full Flag with FE Partial Full Flag. This is the mod I have done
and sent you the ACE file (10_11_06) . Unless this is tested and found to be
ok, I will not be able to implement the rest of the mods.
RELEASED and TESTED at CERN.
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2. Add 8 FE Full Flags to the register in the Special Tracker Header. This
register would indicate that any one FE FPGA buffer has entered the overflow
condition. This needs to be investigated in order to find out how best to use
it to indicate the payload data is corrupt/overwritten. I will try to discuss
with Oz re best way to implement.
Tested at RAL but not released yet.

3. Change BE Status Register Two from 64 bits to 32 bits (already discussed
with JF and Jo).

4. Does JF require a reset sent to the ACE System after a vme reset is
issued? At the moment this is not happening. Need to discuss with JF. This is
to do with problems reading DLY FPGA after an ACE file upload.
UNDER INVESTIGATION (see below)

5. Remove TTC_Ready signal from the BE Command Decoder, as this is redundant.

6. Store the two software DAQ registers in the Tracker Headers in a FIFO at
the time L1A is received (requested by JF).
This is the most complex mod at this stage of development. Therefore all
other mods must be checked to ensure no errors are introduced in the BE f/w
before this change is made.
IMPLEMENTED but not released yet.
```

Event Format changes to word swapping still being considered.

New DELAY FPGA Spy channel with synchronous frame capture tested at CERN. Tracker DAQ want to use this as a monitor to check any problem channels seen in normal data stream. Need to add register to control rate of spy events from FE FPGA. Needs software to unpack data.

Associated change to DELAY FPGA Fine Skew (versions …24 and later) does not seem compatible with FED Industry test software. Timing calibration will be tested at CERN.

Problems often seen when software reloading from SYSTEM ACE CF seen at CERN (Delay FPGAs fail to load). Seems to only happen when loading a new CF file (i.e.. reloading the existing CF file works??). Always works after hardware reset (which implies the CF card update was ok). Can't explain what is happening yet. Can't reproduce at RAL. Suggest repeating with old ACE files, trying with new JTAG term resistors? and test re-inserting CF cards.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Test BLT for System ACE CF loading		JC	01-11-06
Fix Synchronisation problems seen in MTCC	Waiting TOB results.	ST	01-11-06
Decide on event format proposal.		JC	01-11-06
Understand and fix problem with FRL readout.	Done	ST	
Implement DAQ header registers in FIFOs.	Done	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test BLT for System ACE CF loading	JC	01-04-07
Decide on event format proposal.	JC	01-02-07
Suggest shielding scheme on Transition card.	IC	01-02-07
Test CF reloading with old ACE files, resistor terminations	OZ	01-04-07

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 65**		
Project Manager: J. Coughlan **Date:** Wednesday 10 January-2007		**Sheet: 2** **of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05		19.10.06
36	Last FED installed at USC55	26.07.06	01.06.07	
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	