Project Monitor Form

Project: CMS FED **Date:** Tuesday 09 March-2004	**PMF number: 43** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

A total of 40 PMCs have now been sent to CERN completing agreed order.
one sent back from USA already (it got dropped, but likely able to repair).

of remaining 10 :

2 are good spares for CERN;
2 undergoing final test, expect to be good spares.

2 pass all tests, but won't work properly on CERN adapter in PC?
1 is damaged (cap misplaced.)
3 have digital faults, which have not been able to solve.

Propose that Jonathan now looks at about 10 "faulty" cards from previous productions until end of March and then we stop.

FEDv1:

<u>Manufacture</u>

Assembly procedure with DDi has gone well. Very good communications with them.
Started by preparing a list of modifications, do not fits, to go with kitting list (including adding new ADC resistors).

We had difficulty obtaining mechanical samples from Xilinx so gave DDI one of the "dud" boards to do thermal profiling of ovens. They reported that this was invaluable for optimising BGA assembly.

A number of mainly minor snag reports came back. Of which more important were:
Some ADCs got damaged somehow. We had to replace about 80 parts with 40 MHz devices (cf 65 MHz).
TTCrx delivered loose. Will get proper packing from CERN next time. Need baking out.
Plus many small queries showing they really did inspect the kitting and files carefully.

Tests on each board include:
Automated Optical Inspection, BGA Ersascope, BGA X-ray.
Reasonable quote for Takaya flying probe was negotiated so we do this as well (analogue parts).

First 2 boards (13 & 14) were delivered on 8th March (as expected).
Visual inspection at RAL of nr 14 shows assembly quality is very good. Our standard patches have been done and board powered ok in test crate.
Bscan passed with only one error. Dry joint on power pin of one VME buffer chip.

Next step is to load firmware and start readout tests in crate to evaluate analogue build quality.

Remainder 4 boards to come on 11th March, together with X-ray pictures etc.

Other manufacturing news:

One of the dud FED boards was sent to National Physical Laboratory for analysis on 24th February. No news yet.

2nd PCB production meeting with representatives from CMS and ATLAS held at RAL on 3rd March. EU Framework contract for board manufacture advert and questionnaire to be finalised in next 2 weeks.
Atlas 2 CPM boards from DDi also expected this week.

FED Status:

Nr 005 went to PISA after Tracker week FED was integrated quickly and is working. Most of effort at PISA was spent in setting up their XDAQ software.

Second Fed nr 003 is now also under test at CERN. Problems observed in CERN crate. SBS controller went faulty and had to be exchanged. Subsequently FED could not be accessed via VME. Later problem seemed to resolve itself? Checked with JC debug program and it looked fine. Nr 003 often needs explicit power reset button press after crate is powered up.

During Tracker week tests saw occasional errors in fibre header data using recent releases of firmware. Later saw similar behaviour at RAL when using BP clk. Problems cured at RAL with firmware release of 05_03.

Future productions:
Large order (£60K) for Xilinx FPGAs (for min 30 FEDs in 2004) sent out week of 23rd February.

System Tests

S-LINK tests based at Imperial (see talk at this meeting).
Detailed readout tests at various trigger rates and event sizes continue. Actually testing full FED readout chain, not just S-LINK per se.

Some bugs fixed in BE logic, but several problems still remaining.
S-LINK capture can go at higher rate in header recognition mode after BE DAQ header update, improving statistics.
Missing trigger problems now understood as due to APVE.

Problems with fixed rate triggers cured.
Other problems seen when driving Fed with random rates.
Eg FED stopping with (unexpected) FIFO full state.
Also Data lengths from FE's are incorrect sometimes. Don't know if problem is in FE or BE.
Possibly just an artefact of running in scope mode?
Suggest repeat tests with Frame Finding rather than Scope mode (i.e. in proper data readout

mode).

Results are trying to be understood and correlated with buffer status bits and FED counters.
APVE has to handle FED throttle signals to run at high rates. TTS signals added to BE FPGA.

CERN state that DAQ link cards will handle 80MHz transmission up to 10 metres.

FE FPGA algorithm tests at RAL (see talk at this meeting):
PPD has shown that ZERO SUPPRESSION in FE FPGA is basically working.
Some minor "features" uncovered. Bad strips can only be suppressed in pairs (except at edges)?
Ordering of fibres for data complementing function is unexpected. Single strip hits ignore high threshold if low cluster threshold set to zero.

Other Tests to do…
Power and currents driving all 96 inputs in progress at Imperial.
Test of Temp cut out and Hot Swap at RAL (needs patch to board).
TTC commands, resets etc.

<u>Firmware</u>

Delay-FPGA:

FE-FPGA:

Some time was spent studying cause of format errors in fibre headers. Eventually appeared to be correlated with changes to FE DCM logic a few weeks ago. Logic is now sorted out since version FE_02_15. No errors seen since and raw data captured from OptoTester is also ok.
Problems synthesising on new PC resolved as due to incorrect environment variables for tools.

BE FPGA:

Mainly debugging of logic for S-LINK readout. Adding additional status bits to detect overflow conditions etc.
Header and trailer formats changed to match latest DAQ descriptions.
Implementation of full state machine TTS signals is in progress (for APVE interface). Keep separate throttle lines for CERN tests.

Also need to implement TTC chan B serial decoding (and understand how to drive TTCvi to generate commands in first place).

VME FPGA:

ADM voltage monitor is implemented and tested. Allows monitoring of all crate supply and derived voltages (and a few other bits and pieces).
LM82 serial interface for temp monitoring is implemented and tested

System ACE controller interface is implemented and tested. VME 03_0F
Major step achieved. Succeeded now in reprogramming contents of Compact Flash card in-situ. (most of work in software).

Other Issues

Review of FED URD.
First pass done between Ian T. and John C see URD v0.54
Second pass after this meeting.
Also need to amend FED deliverables spec document (e.g. change in responsibility for final software, transition card for s-link, tts signals).

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Update project pages for internal audit.	In progress	JC	27-02-04
Test access to System ACE registers.	Done. Including reloading CF.	ST/JC	
Manage assembly and delivery of 6 more FEDs to RAL.	Done. 2 at RAL. 4 more this week.	JC	
Arrange to send bad FED to NPL	Done.	JC	
Prepare order for further purchase of FPGAs	Done.	JC	
Complete delivery of 40 PMCs to CERN	Done.	JC/JG	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Update project pages for internal audit.	JC	31-03-04
Implement and test TTC chan B.	ST/JC	26-03-04
Sign off new project deliverables with customer.	JC	26-03-04
Test next 6 FEDs.	IC/JC	19-03-04
Get S-LINK working with random triggers.	ST	26-03-04

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 43**		
Project Manager: J. Coughlan **Date:** Tuesday 09 March-2004		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.5**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
17	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
18	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
20	New version OptoRx at RAL	01.04.03		21.07.03
21	FEDv1 Interim Review	08.09.03		11.09.03
22	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
23	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
24	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
25	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04	11.03.04	
26	Finalise design changes for FEDv2	01.04.04	30.04.04	
27	Design Review FEDv2	30.04.04	01.06.04	