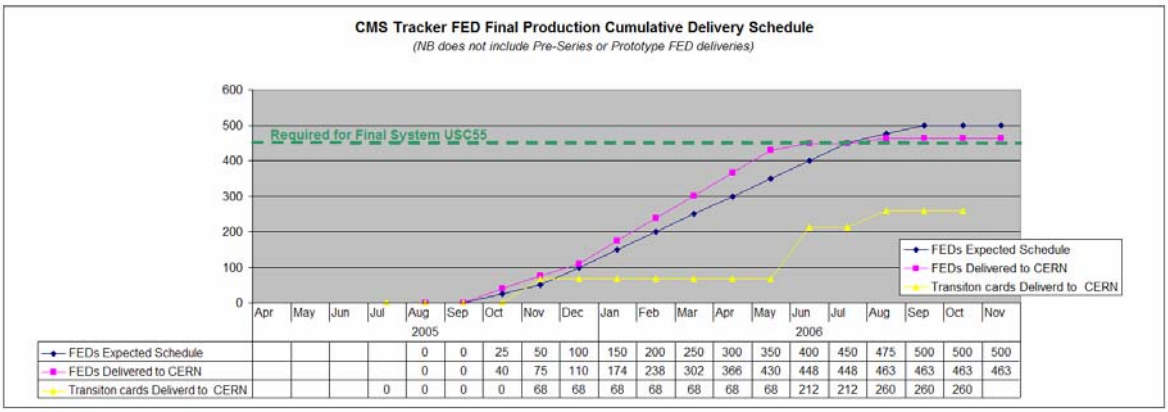
Project Monitor Form

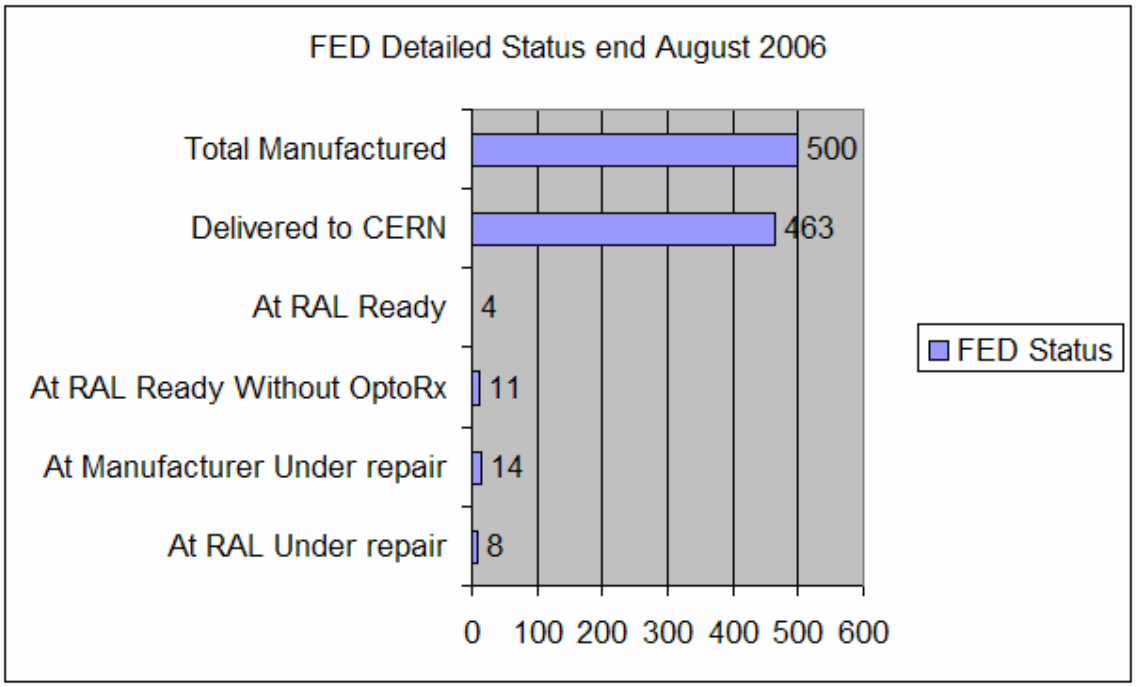
Project: CMS FED **Date:** Friday 8 September-2006	**PMF number: 63** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production



	Aug 2005	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun 2006	Jul	Aug	Sep	Oct	Nov
FEDs Expected Schedule	0	0	25	50	100	150	200	250	300	350	400	450	475	500	500	500
FEDs Delivered to CERN	0	0	40	75	110	174	238	302	366	430	448	448	463	463	463	463
Transiton cards Deliverd to CERN	0	0	0	68	68	68	68	68	68	68	212	212	260	260	260	



further details in Production spreadsheet.

Disk crash on RAL test lab PC. Took about 1 week to recover working test system with SBS bridge (with help from James Leaver)
But still haven't got the CAEN bridge working again.
We now have a RAL backup!
NB systems at assembly plant always had a backup disk.

Further 3 boards returned from CERN. 1 pre-series fixed. 2 under inspection.

SLINK Transition Card

- All cards have been delivered to RAL.
- 260 tested cards have been sent to CERN.
- Yield very good. ~ 6 out of 280 have failed test. But expect most will be simple to repair.
- Expect to send 450 tested cards by beginning of November. Spares later.

Oz had mechanical problems fixing screws for CMCs on 3 of 260 delivered Transition cards. Put to one side.

CERN USC Installation and Commissioning :

Oz has released a preliminary installation schedule.
Depends on availability of final crates. But should aim to install at least one existing crate of FEDs in USC by late Oct / early Nov if rack services and safety systems are all operational.

Will organize RAL engineer visits when installation dates are fixed.

Ivan has sent Oz requested equipment CERN for installation and has most of remaining parts, e.g. JTAG cards, ready at RAL.

Karl is coordinating cabling of Tracker. Propose Jo to act as single point of contact for FED.

Ivan has ordered 400 Front Blanking panels. Will be delivered direct from manufacturer to CERN. About 50 already received.

Ivan has updated Oz's crate list with RAL information.

System Integration Tests

TIF : Status of optical cabling of FEDs to Tracker in B186 uncertain.

MTCC Reported issues :

Synchronisation problems when recovering from runs aborted by the DAQ (aborts for reasons unrelated to Tracker). Sometimes in the next run the DAQ FRL receives unexpected event number from the Tracker FED. Suspect this is due to FED buffers not been flushed correctly at the end of run. Saeed suggested a better mechanism for flushing. This had some success, but problems are still observed.
In order to diagnose this condition RAL has requested further information on FED counter status and event header contents during these problem runs.

The DAQ register which holds on the fly run status information in event header is not being updated as expected. Suspect Tracker DAQ is trying to change register during the run. This can lead to unspecified behaviour.

Mystery counter resets. These only seem to happen intermittently in 904 lab? Suspect TTC setup is different?

Firmware :

New SPY channel synchronized to Frames has been implemented in Delay chip. Ready to test with new FE next week.
NB This design needs updated software for finer resolution delay skews before it can be used with Tracker DAQ.

Software proposal to reorganise formats to match software processing.
Event format word swapping. Event formats in SLINK and VME readout appear different in software memory. However at the FED output the word ordering is the same. Suspect swapping is happening in VME bridge.
Pros: Faster offline processing of events, but the gain has not been quantified?
Cons: Probably difficult to implement in Firmware. Testing and bug fixing effort. Changing a standard working since 3 years. No guarantee that final SLINK chain won't upset ordering again.
Conclude: Proposal needs a lot more consideration.

Software :

Gareth Rogers has implemented many new features in online software. Updated version of relevant documentation is released.
CF Firmware loading for multi-FED system has been tested successfully. But need to improve speed. RAL to investigate.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Send TTCoc files to Jan Troska		IC	01-03-06
Implement SPY mode in Delay FPGA	Ready for testing.	ST	
Implement additional status word in BE header	Done	ST	
Fix html files at eXception		JC	01-07-06
Add partial empty, half full flag register	Done	OZ	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Send TTCoc files to Jan Troska	IC	01-08-06
Fix html files at eXception	JC	01-10-06
Complete delivery of 450 Transition cards to CERN.	IC	01-11-06
Test BLT for System ACE CF loading	JC	01-11-06
Fix Synchronisation problems seen in MTCC	ST	01-11-06
Decide on event format proposal.	JC	01-11-06

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 63**		
Project Manager: J. Coughlan **Date:** Friday 8 September-2006		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05	01.11.06	
36	Last FED installed at USC55	26.07.06	01.06.07	
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	