Project Monitor Form

Project: CMS FED	**PMF number: 54**
Date: Friday 8 Apr-2005	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

Manufacture of Pre-series
Production of **5 + 20** off FEDv2:

Limited work has been done on faulty boards, which have rather been put aside for later investigation and we move on to the next batch....

First 5 :
3 pass all single board Acceptance tests. (1 is at CERN and 1 at Imperial.)
1 has one dead channel on an ORx output
1 with one damaged FPGA rework completed to return next week

Last 20 :
10 Delivered to RAL on 9th March , remaining 10 on 18th March.
12 pass all single board Acceptance tests (incl Optical inputs).
2 are almost working
1 appears to have no outputs on one ORx
3 have power problems
2 have Boundary scan problems

So we would have enough to start Full Crate Tests now as anticipated.

Air deflector bars should arrive this week.
We have arranged for unused kit to be returned to RAL.
We plan to hold a pre-series review meeting at eXception plant at the end April / early May.

Other boards

Second of original pair of FEDv2 boards nr 019 was sent to CERN on 7th March.

Re FEDv1s

Nr 005 and 013 were upgraded to v2 compatible*. Full functionality except no SLINK.
Nr 013 was sent to CERN yesterday.
Nr 005 appears to have one dead channel on an ORx output (otherwise ok)

*** ACE File: 04_03_05 ; EPROM : VME_03_1b**

Design Testing :

Further extensive tests of high rate S-LINK Zero-Suppressed readout on FEDv2 boards continued to show at relatively low rate (few per hundred million) of CRC errors (at high occupancies > 8%) on the Imperial rig. These problems were never seen at RAL using same firmware and test software.
Before Easter the SLINK kits were therefore exchanged. The same level of CRC errors is now

observed at RAL, and none at Imperial, i.e. the problem moved with the slink kit. However, it did not prove possible during this investigation to isolate any particular element of the link kit as the cause.
(NB these errors have also never been seen with VME event readout).

In order to increase our flexibility with the SLINK we are also implementing firmware to allow the SLINK clock to run at other values than current 80MHz (although rate is still fixed in firmware). If the problem is sensitive to the timing on the link then e.g. running at 40MHz should cure the effect.
NB The final long 8-10m cables discussed by the DAQ group are NOT compatible with the connectors on the SLINK FED Kits. So we must rely on the DAQ group to test with long links.

VME Block Transfers: Observed that sometimes BLT readout fails when FED is in right most slots in crate. Other times it works fine (x10 faster) as expected? CERN results show a correlation of BLT problems with the type of SBS interface i.e. electrical or optical. Difficult to investigate this in FED Tester crate. Very interested to see how they behave with CAEN controllers.

ORx/Analogue

Stefanos Dris at CERN tested approximately 12 channels on the FEDv2. The results are what were expected from the modified FEDv1 tests. There seems to be no degradation in dynamic performance due to the lower resistor value 62 Ohm. He may test more channels to obtain more statistics, but he has seen enough to recommend freezing these values. Francois Vasey and Jan Troska have seen the results, and concur with this conclusion.

Francois has still to sign off FEDv2 Orx/Analogue design.

Firmware :

BE FPGA:
Labelling of TTC calibration events in DAQ header during normal runs is now working.
Some additional firmware for error checking on BX synchronisation is now being tested.
SLINK output rate adjustment is being implemented (see above).
An annotated list of low-level software needed to exploit many new BE FPGA firmware features was released last week after discussions with Matt.
Otherwise all the BE specific remaining requirements are completed (although some effort will be needed to interface the new features in the FE FPGA below).

FE FPGA:
Osman now has a VHDL version of the FE FPGA design which tests show functions as the VERILOG original (see report at this meeting).
Most of the remaining requirements to be implemented require modification in the FE design (see annotated list presented at last meeting).
It is proposed to adopt the VHDL version as the baseline design code for these changes as the use of VHDL code should assist long term maintenance.

<u>Final Acceptance Testing</u>

The spare LHC crate was tested successfully with a FED during CMS week. It will be dispatched this week. An extender box to interface to the SLINK PC is also being sent. This

needs testing at RAL.

Jan is going to test a FED with a new Optical splitter board to verify that our present multimode TTC pigtails will function with the single mode fibres proposed for the local distribution system. After this an Optical splitter can be sent to RAL for use in the Full crate tests.

Greg is testing a new adapter card to interface the FED Testers to the TTC system. This will allow multiple a full crate of FEDs to be driven simultaneously. See report at this meeting.

Assembly Plant Testing

Test engineers from eXception spent another day at RAL just before Easter. They were taken through the testing of some of the pre-series boards to gain experience of the procedures. The discussions and their comments were very positive. They have suggested some simplifications.
2 x JTAG/Boundary scan kits were ordered and have just arrived.
Some further improvements made in LabView app related to transfer of BScan files and storage of test results in EPROM.

Final Production:

Papers were prepared for the CERN Finance Committee in March. But it was later decided by CERN management that it would not be necessary to submit them. Tony Wells, of RAL contracts, is in contact with Achille Petrilli to organise the transfer of CMS funds for the final production contract. A project code is being set up in EID to hold the monies.

A meeting to discuss the final contract with eXception EMS management was held at RAL on March 21st. Most issues related to the contract are agreed in principle. In particular, the companies proposed payment schedule would be satisfactory. The delivery of 50 boards per month was agreed. A contract document, based on the EU Framework tender, is being drafted.
Subsequent to the meeting, a final Bill of Materials was released taking into account the RAL free issue items and with the same Xilinx FPGA pricing we obtain from our distributor.
The BoM also explicitly listed the long lead (8-14 week) components. An order is being placed to purchase these parts, in advance of agreeing the final contract, in order to avoid additional delays in the production schedule. This sum would be deducted from the first payment to the company.
Final discussions are taking place concerning the cost of handling our free issue components, in particular the ORx, which are now the dominant material cost.
A fall back option of assembling the ORx ourselves, most likely at Imperial, is being considered.

Forward Look

Activities, objectives and resources for the next 6 months are to be discussed at this meeting…

- Production and acceptance tests in UK.
- How do we exploit/contribute to B904 integration centre?
- Remaining Firmware requirements and associated low level software.
- Higher level software tasks , calibration, run initialisation procedures …etc
- +++

CMS schedule has Nov 1st 2006 as milestone for delivery of Tracker ready for installation. Our objective is for all final system FEDs to be installed in USC55 and operating with test data to the DAQ system (whatever is available to us) by this date.