Project Monitor Form

Project: CMS FED	**PMF number: 41**
Date: Thursday 08 January-2004	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

PMC test bench back in action.
Also modifying the last batch of 10 cards (nrs110-119, spare pcbs and last time buy component cards).
A further 6 PMCs are now ready (just need a final test in Linux box).
3 PMCs from USA expected back today for resistor mod.

FEDv1:

Manufacture

Following decision at last meeting a further 6 (+1 spare PCBs) are in production at DDi (same pcb company used by CALICE). Expected delivery date is 14th January. Metal finish is Nickel/Gold as requested.
Board impedances changed slightly (single 56->60 ohm, diff still 100 ohm), but it can be compensated by other standard resistors.
Component kits ready. Assembly to be done again by SAETech.

Also investigating one stop shop companies for a subsequent production of 4.
Visit to Cemgraft (FED-Tester assembler) arranged (provisionally 15th Jan) and DDi soon after.

Second FED for CERN:
All channels on nr 003 were modified and tested using OptoTester. 4 faulty channels were fixed (all minor repairs once diagnosed). Minor mod to ensure clean power boot up. Event readout checked.
Shipped to CERN on 19th December. No word yet from CERN of receipt.

FED rework at Imperial:
Based on original Bscan and Ersascope had selected 006 and 007 for rework.
Later found unexpected readout errors (eg wrong bit patterns) when testing on nr 007. Not explainable by original Bscan.
Tried to repeat Bscan on nr 006 and 007, but they will not now power on the bench (ok in crate?). So cannot be confident which BGAs need attention. Can't recommend rework.

Fitted Front Panels so Nr 006 and 007 can be used for power tests at Imperial (3 cards in crate). All FPGAs on these 2 FEDs load up so give realistic power measurements.

New summary spread sheet of FEDv1 status made.

Components:
9Mb QDR memories from Micron are now obsolete.

Enough in hand for next 6 FEDs. Can buy enough for a further 20 now.
Investigating alternatives.

System Tests

Still can't get 2 SBS cards to work in one PC (to conveniently exploit the LHC crate). This should work, but CERN experts haven't tried it.

Power measurements:
Good news. Achieved a reduction in 3.3V current demand of between 3 and 4 amps by disabling Digitally Controlled Impedance on Delay FPGA outputs pins (96 x 5 pins). DCI is not needed here.
Updated current estimates and measurements spreadsheet.
Measured currents per board (but without inputs) are safely within pin limits. Also within crate limits for 20 FEDs assuming we can have 300A limits on both 3.3V and 5V
NB Important to measure when driving all 96 inputs hard and with various OptoRX settings (Imperial).

S-LINK tests at Imperial:
Had hoped to use nr 007 for these (but see above).
Have modified nr 002 to provide power to transition card.
WARNING: BE FPGA firmware has now been changed to match Transition Card use of pins. Older firmware versions should NOT be used on **nr 002** or there is a risk of damage to FPGA.
Nr 002 recently had 4 OptoRx fitted. Input channels are not all checked. Digital functions ok except TTCrx doesn't work. But fine for S-LINK tests.
NB This leaves only one working card nr 004 at RAL.

Zero suppression tests at RAL:
PPD testing of re-ordering and pedestal subtraction logic in FE FPGA using FED-Tester input data patterns. Need to concentrate effort to verify logic in next 3-4 weeks.

CERN tests:
Nr 005 report stable operation of FED over several million events.
Hardware throttle also now used.

Firmware

Update of firmware set released to Imperial and CERN on 18.12
Improves clock handling and fixes a few reported bugs (see details below).

Delay-FPGA:

Spy Channel testing has started, but needs debugging.
Observe correct length of spy data, but all zeroes.
Need assistance from Ed Freeman who is not back from leave yet.

FE-FPGA:

Chans 9&10 could not be changed to 1Vpp mode. Problem was misassigned pin. Fixed.

BE FPGA:

Optional pattern generator useful for S-LINK test has been implemented. Replaces Front End input data.

VME FPGA:

Clock re-setting and error recovery have been improved (see relevant e-mail).
Mods needed to readout spy channel implemented, but not working yet. Problem may be in Delay FPGA (see above).
Interface to serial EPROM (for storage of ser nr etc) is well advanced.