Project Monitor Form

Project: CMS FED **Date:** Thursday 07-March-2002	**PMF number: 11** **Sheet:** 1 **of** 2

Project Implementation phase.

News and comment

Customer has asked us to investigate option of producing FE Module analogue circuit on pcb for evaluation of design with OptoRx at CERN.

Manufacture:

Chris noted that 12 layer board with controlled impedance would require 2mm thickness. This may necessitate special crate runners or the milling of edges to fit standard VME crate runners.

Front End Module:

Following tests and simulation studies of analogue circuit James has identified a problem with generating VREF. This is a consequence of fundamental challenge of converting unipolar single-ended OptoRx signals to bipolar differential with a different common mode voltage for the ADC. He is now investigating various solutions to this problem.

James has also selected a component (National Semiconductors LM2) to monitor temperature for OptoRx and FPGA diode.

CERN have requested to manufacturer OptoRx final pinout changes (as suggested by Adam.)

John brought back an OptoRx module (mechanics only) from CERN.

Chris is continuing with entering components in library.

Firmware:

<u>Delay FPGA</u>:

Ed is finalising the FPGA pinout and associated components for Chris/Adam.

Spacing between delay FPGAs is tight at limit of 2mm. May have implications for ease of inspection and reworking if required.

Board level:

Saeed has completed the table of current and power requirements for FED. The estimation for FPGA consumption was based on realistic design simulations but implemented on VirtexE (VirtexII consumption should be lower.) He noted that FPGA consumption varies enormously depending on design.

Other Issues:

Actions from the previous PMF

Action	Status	Who	Target date

Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	In progress	EF	31-02-02
Produce pinout of Delay FPGA for inspection by Adam.	In progress	EF	11-02-02
Make request to R. Stephenson to borrow simulations tools license for James's PC.	On going	RH	11-02-02
Produce proposal scheme and devices for temperature monitoring of OptoRx and FPGAs.	Done	JS	
Produce 1st order FE module analogue component layout.	Opamp section to be modified by James. Remainder ongoing.	CD	25-02-02

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Test independent 360 degree phase control on 4 DCM channels of delay FPGA evaluation board. Tabulate results of measurements.	EF	11-03-02
Produce pinout of Delay FPGA for inspection by Adam.	EF	11-03-02
Make request to R. Stephenson to borrow Orcad professional simulations tools license for James's PC.	RH	11-03-02
Produce 1st order FE module analogue component layout.	CD	25-03-02
Find out from Paul Hardy whether it is possible, and if so how, to automatically generate Xilinx FPGA symbols in CADENCE.	RH	11-03-02
Propose FED power distribution scheme following standard LHC crate PS specifications.	ST	18-03-02

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** R. Halsall **Date:** Thursday 07-March-2002		**PMF number: 11** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.0**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	**Project Spec sign off**	**21-12-01**		**05-02-02**
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	11-03-02	
5	FE Module Feasibility Review	28-02-02	11-03-02	
7	**Board Level Feasibility Review**	**04-03-02**	**08-04-02**	
8	Delay FPGA Interim Review	31-01-02	04-03-02	
9	Front End FPGA Interim Review	31-01-02	04-03-02	
10	Back End FPGA Interim Review	31-01-02	25-03-02	
11	VME FPGA Feasibility Review	28-02-02	25-03-02	
12	Clock FPGA Feasibility Review	28-02-02	25-03-02	
13	Release Test Plan Document	22-02-02	08-04-02	
14	FE Module Final Review	30-04-02		
15	BE Board Final Review	10-05-02		
16	Full Board Design Final Review	31-05-02		
17	**IDR Customer Production sign off**	**10-06-02**		
18	**Batch 0 (2 off) Non-Opto Assembled boards at RAL**	**26-07-02**		
19	OptoRx for Batch 0 at RAL	26-08-02		
20	**Batch 0 Opto Assembled boards at RAL**	**01-11-02**		
21	Batch 0 review	06-01-03		
22	**Batch 1 (8 off) Assembled boards at RAL**	**21-03-03**		
23	**Delivery Batch 1 to CERN completed.**	**11-07-03**		