Project Monitor Form

Project: CMS FED **Date:** Monday 07-January-2002	**PMF number: 03** **Sheet:** 1 **of** 2

News and comment

Not much to report since the previous meeting owing to long xmas vacation period of several team members.

Feasibility Study continues

Planning:
Awaiting approval of Project Spec from Rob before releasing to customer.

Front End Module:
Chris is now available to start work on CMS layout. He will work with James to investigate problems of attaching simulation models to symbols under AWB.

Firmware:
Ed has fixed the problem with the reset condition and can now start testing the clock delay design on the Virtex II 40K evaluation board.

Azmat is due to go on leave today for 3 weeks. He will meet today with Rob and Saeed to discuss the hand over of the BE FPGA design.

Other Issues:
The mis-assignment of staff effort on the CMS project code is persisting despite complaints.

Actions from the previous PMF

Action	Status	Who	Target date
Develop draft schedule	In Progress	JC	xx-01-02
Produce procurement list for 9U Prototype	In Progress	JC	14-01-02
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	Ongoing	RH	17-12-01
Organise hand over meeting for Back End FPGA	Ongoing	RH	19-12-01
Organise a Board Level Design Meeting	Ongoing	RH	20-12-01
Pass schematic for Analogue part of Front End module to DO	Ongoing	JS/CD	17-12-01
Test key aspect of Delay FPGA on development board in Lab	In progress	EF/RH	31-01-02

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Approve draft Project Spec & FED prototype costings before customer meeting.	RH	10-01-02
Develop draft schedule	JC	14-01-02
Produce procurement list for 9U Prototype	JC	14-01-02
Check Impact Memec if Cadence Xilinx footprints/symbols exist on Xilinx Web site	RH	14-01-02
Organise a Board Level Design Meeting	RH	14-01-02
Organise hand over meeting for Back End FPGA	RH	14-01-02
Pass schematic for Analogue part of Front End module to DO	JS/CD	14-01-02
Test key aspect of Delay FPGA on development board in Lab	EF/RH	31-01-02

Project Monitor Form- milestones

Project: CMS FED **Project Manager:** R. Halsall **Date:** Monday 07-January-2002		**PMF number: 03** **Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02	14-01-02	
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	