Project Monitor Form

Project: CMS FED	**PMF number: 49**
Date: Monday 6 Sept-2004	**Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

First 2 FEDv2 boards (ser nr 18 & 19) arrived on August 2nd as expected.
Unfortunately PCB was made using ODB++ files sent for quotation purposes rather than final design files.
Fortunately only one minor difference between 2 sets, which was easily patched.
DDi admitted fault was on their side. Procedure has been put in place to avoid repetition of mistake.
Otherwise production went through with only minor snags.

Both boards powered up first time.
Boundary Scan passed. JTAG configuration set up needed some adjustments for new connector wiring and inversion of TTCrx rst. Latter caused many Bscan errors until spotted and confusion was compounded by use of TTCrx v3.2 chips.
Analogue tests showed problem on group of 4 chans on nr 19. Cured by replacing one Faulty OpAmp.
Digital tests show problem on Temp sensor attached to BE FPGA on both boards.
Basic VME readout working.
Evaluation now continuing after summer break.
Route cards will keep list of all faults as usual.

Note: These 2 PCBs are 1.8 mm “standard thickness” (c.f. 2mm for FEDv1). This is likely due to new build using DDi rules. Ok in LHC crate slots.

QDR memories:

A BSDL file for the new Samsung QDR memory device was finally obtained. Following further tests including boundary Scan and Ersascope inspection we are satisfied that the address problem on Board nr 12 with new QDR is due to failure in rework of the BGAs (even though great care was taken).
An order for final FED production quantity of these QDRs (MoQ ~ 2000) was placed this week. Lead time of this device (12-14 weeks) will likely determine pre-production schedule. Other parts are in hand.
Provisional slot arranged with DDi for next batch of 20 FEDv2 in November.

FEDv1:

Testing :

CERN reported on a degradation of the OptoRx settling time by the FED front-end. To reduce the settling time Mark Raymond suggested tuning the value of the existing cap across the input to the ADC (latter should not to be confused with “peaking caps” which were removed from

FEDv2 design). It was agreed with CERN that for each of 3 values of Rload several standard cap values would be fitted on different channels on one of the boards at Imperial (ser nr 02) . This board already has OptoRx having internal capacitance adjustment. This board would then be sent to CERN to have the tests repeated.

High random trigger rate tests at Imperial show agreement with original buffer occupancy simulations made by Emlyn Corrin.
But in high rate S-LINK readout have observed a low level (1 per million) of events with incorrect total length in ZS mode (this effect is not seen in Scope mode). Not able to capture dumps of these bad events yet.

Firmware :

Problem of occasional apparent FPGA load failing has been cured (bit file load was actually completing but subsequent FPGA start up was failing). Followed Xilinx trouble shooting suggestions by speeding up Done signal.

New standard release of FEDv1 Firmware released which cures the major readout format error (frequent missing word at start of tracker payload) which was observed in last beam test.

ACE File: 16_07_04_1500 = (Delay 02_1B ; FE 03_16 ; BE 02_43)
EPROM : VME_03_0F

Discrepancy (few percent) reported at CERN between S/N measured in ZS mode and Raw Data may be due to incorrect handling of negative CM noise in FE FPGA. This has yet to be looked at in detail.
Suggest normalising pedestals (by subtracting an offset common to all strips) before loading into FED to cure this problem? This is implicit assumption of FE FPGA logic.

Proposal for codes for TTC chan B commands has been agreed.

Currently migrating all 4 FPGA designs to latest release of FPGA tools. This is time consuming but necessary, as support for currently employed tool set is now limited.

We want to make FEDv2 design the standard FED as soon as possible.
FEDv1 boards can be upgraded so that Firmware HDL source is compatible with FEDv2 with simple addition of couple of LVDS clock resistors. This is already done on all boards at RAL. Propose to do this to all boards at CERN after the beam test.
Consequence is we freeze last release of firmware for FEDv1 for next beam test (see above). Firmware Bit Files in Compact Flash for FEDv2 will of course be different from FEDv1 due to new pinouts but this will be transparent to end users.

Software :

Gareth Rogers documented the Low level FED software and associated standalone test software before he left RAL. He also integrated the code into Greg's Tester Utilities. Responsibility for this code is handed over to Matthew Pearson.

Standalone test suite for Assembly plant testing (based on LabView calling C++ code) is well advanced. An updated list of manual operations on FED boards has also been incorporated.

The test suite was ported quickly to RAL and is already up and running on the new FEDs.

Other Items

50 FEDv2 front panels in hand (10 were finally sent to Francois this week).

First 6U Transition cards are now under test at Imperial.

NB Propose to adopt the new FEDv2 numbering scheme for FE FPGAs (with #1 at bottom and #8 at top). Should we re-label FEDv1s?

LECC Boston takes place week of 13th September.

Next beam test starts late September. Plan for RAL engineers to visit for couple of days.

Tender :
Invitation to Tender document (with FED as one of quotes) prepared. Small print is still being worked on by RAL Finance.