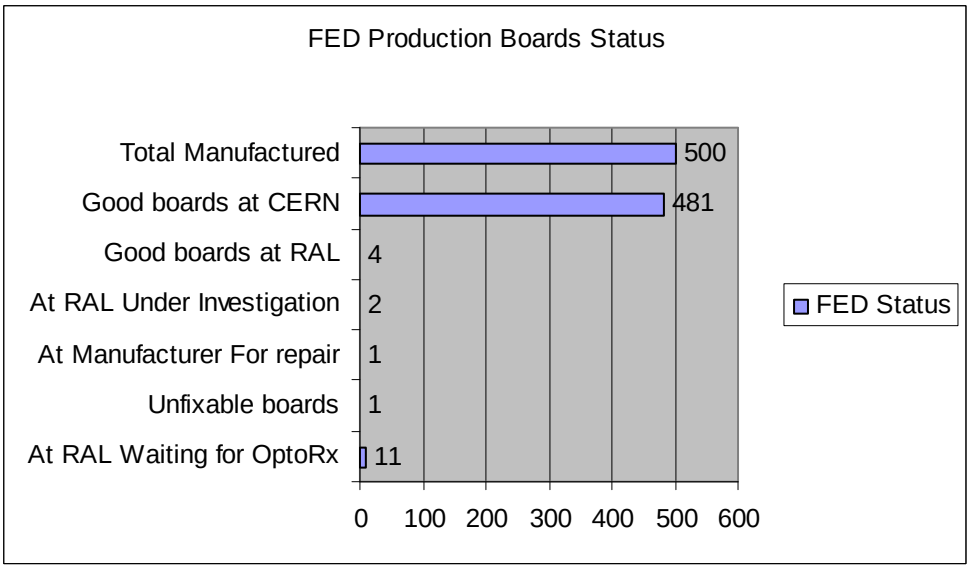
Project Monitor Form

Project: CMS FED **Date:** Wednesday 6 June-2007	**PMF number: 67** **Sheet:** 1 **of** 2

Project Implementation phase.

FED Production

A further 16 FEDs have been delivered to CERN.



Full details in Production spreadsheet.

FEDs

Exception have now cleared the backlog of board repairs.
Ivan is in process of recovering ORx from only unfixable board.

Of the 5 boards returned from CERN so far: 3 have had faults identified (all different) and have been repaired ; cannot find any problems with remaining 2 boards (will return both to CERN and retest during Ivan's next visit).

CERN Contract

FED production code RQ09600 has been closed and balance of £24,735 transferred to FK50800.

CERN Installation and Commissioning :

A total of 306 FEDs are installed at USC with SLINK connections.
Awaiting tests with DAQ using fake data.

No more news on any rack grounding scheme changes.

Cooling related problems observed in TIF. Some FEDs were shutting down with over temperature.
Flexible pipes between manifold and cooling units were cleaned out. Found a lot of gunge inside. Waiting to see if this cures problem.
In parallel investigating ways of mitigating against cooling system problems on the FEDs by adding heat sinks to a couple of hottest ORx (see below) and installing blank cards (rather than just blank panels) in some slots.

Hi Jonathan,

I have managed to remove the copper heatsink from the FED in 904 and measured the LM82 temperatures with the same FED and crate.

FEDs in crate cmstracker003 : slot 3,4,5 10,11 with TTCoc in slot 9 Bin temperature: 23C FED hardware id: 38 in slot 10

Temperatures in slot 10:

Opto-Rx	With Heatsink	without heatsink
8	38	38
7	49	54
6	56	61
5	52	56
4	45	46
3	36	36
2	33	33
1	31	31

As you can see, if the bin temperature remains contant there is a decrease of 5C.

Thanks,
OZ

SLINK Transition Cards

First batch of ~ 70 cards from CERN had shielded RJ45 connectors fitted (at Cemgraft) and have been returned to CERN.

Firmware and System Integration Tests

Generally the ~ 3 crates of FEDs have performed reliably during the TIF cosmic runs.

100kHz noise effects still seen in module tests at CERN. Now confirmed using Raw Data readout with new event downscaling option implemented in FE and BE firmware.

Problems “reported” with FEDs shutting down at run initialization during ORx setting adjustments? Is this related to TIF cooling issues?

Jon reports event data corrupted on a couple of FEDs during TIF runs. Oz will check these at 904.

Event Format changes to improve Filter unpacking efficiency. Necessary changes to BE have been investigated. Tests at CERN reported a 6 x increase in unpacking speed?? But this is not confirmed.

New DELAY FPGA Spy channel data with synchronous frame capture has now been verified against raw event data readout at CERN.

DELAY FPGA Fine Skew 64. Have observed “noise” during timing calibration runs on some FED channels (maybe a pattern exists). Suspect new firmware may have fitting problems.

New FPGA Compact Flash card updating software uses multiple threads to carry out parallel loading of all FEDs in a crate. On one occasion an accidental interruption of the process caused the corruption of all cards in FEDs in crate and necessitated physically removing and reprogramming all the compact flash cards (and of course FEDs).

No more news on other CF card file problem reloading problems.

Documentation

The new Delay FPGA Technical document was released.

A major revised version of VME FPGA Technical document has been circulated for comments.

sLHC

2nd CMS UK upgrade meeting held at RAL March.
CMS UK will submit a bid to grants committee in September. It was agreed to merge existing drafts for new FE chip (Mark Raymond) and off-detector readout work packages into a single Readout work package.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Test BLT for System ACE CF loading	No longer required.	JC	
Fix run start problems seen in MTCC	Likely due to SLINK initialisation sequencing.	ST	
Test CF reloading with old ACE files, resistor terminations	Problem no longer reported.	OZ	
Test CF reloading with old ACE files, resistor terminations	Problem no longer reported.	OZ	
Provide draft of work package for FED SLHC upgrade	Done. Will now be merged with FE chip work package.	JC	
Find out what has happened to boards under repair at Exception	Done. Boards repaired.	JC	
Implement new Event Format and Test with memory dump	Done.	JC	
Update fedDebug program to process new Event Format	Not urgent	JC	30-03-07
Send 16 good FEDs to CERN	Done	IC	30-03-07

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Fix noise problem with new Delay Fine Skew 64	ST	30-06-07
Move ORx from bad board to unpopulated Fed.	IC	30-06-07
Release new VME FPGA document	ST	30-06-07
Test new heat sinks on ORx	IC	30-06-07
Update fedDebug program to process new Event Format	JC	31-07-07
Merge work package for FED SLHC upgrade.	JC	30-06-07

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 67**		
Project Manager: J. Coughlan **Date:** Wednesday 6 June-2007		**Sheet: 2**	**of** 2	
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Sign Tender contract	09.02.05		24.06.05
31	FEDv3 tape-out	06.04.05		08.06.05
32	First FEDv3 boards at RAL	13.07.05		28.07.05
33	Production of 500 FEDv3 starts	08.09.05		01.08.05
34	First FEDv3 at B904 Prevessin	30.11.05		27.10.05
35	First FED installed at USC55	17.11.05		19.10.06
36	Last FED installed at USC55	26.07.06	01.06.07	
37	Power on Tracker at USC55	01.08.06	01.07.07	
38	Readout test with Tracker at USC55	01.10.06	01.08.07	
39	LHC test run	02.04.07	01.11.07	