Project Monitor Form

Project: CMS FED	**PMF number: 26**
Date: Wednesday 05-March-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

Status:

Testing on ser 001.

Learnt how to use ChipScope tools for analogue tests.
Single channel tests until cross-point switch test card is available (see below).

Added test connectors on FED behind OptoRx.
Input signal generator signals through test connector.

NB with no input all ADCs should read '0'.

Verified input voltage ranges/analogue default settings are as expected.
Sine wave input 0.5 -> 1.5V matches full range of ADC.

Apply reference value of 1.0 V to see pedestal. Observed noise at 10 mV level. Same effect on several channels.
Main effort to investigate possible noise sources.
Probable candidates are crate PS @ 90 kHz and one of DC-DC switchers on FED @ 500 kHz.
Has effect on DAC output to OpAmp, which feeds directly into signal.
Now studying effect of filers on switcher and caps on DAC outputs.

(Hold off plan to assemble 3rd board (without FPGAs) for advanced Power circuit testing whilst noise investigations continue.)

Modified test firmware to permit deeper chip scope captures (4K samples max.)
Need to move chip scope from Delay FPGA into FE FPGA for very deep capture.
Try final design in Delay FPGA to test DDR transfers.

In any case would like to test for any effects on analogue signals with more realistic designs running in FPGAs.
Eg See noise spike on signal when a "reset" is sent to Delay FPGA. Could be caused by resetting of Digital Clock Managers (not a problem in normal operation.)

Still investigating why ADCs run hot until FPGAs are programmed? Less important now that CFlash loading is operational (see below.)

Digital tests going in parallel with analogue testing.

Xilinx eventually provided a "work around" for problem of creating configuration files with more than 30 devices. Problem was in GUI tools. Use batch version of tools and create an intermediate SVF file.
After doing this were able to generate a System ACE file describing entire FPGA chain. Now

tested SystemACE on FED. Board loads on power on from Cflash card and takes approx 20 secs. (c.f. 3-6 mins with cables.) (could be made even faster by increasing clock speed from 10MHz.)
NB JTAG jumper settings on FED need to be adjusted to use System ACE, but this is a one time operation. NB Keep parallel cable attached for ChipScope readout and VME FPGA EPROM programming.

Earliest completion of (very) basic analogue tests at RAL on first board was end of this week (10). We would like a further week (11) to continue analogue tests with new test cards before deciding on OptoRx assembly.

Electrical Test Card:

Used for multi-channel FED electrical tests.
First 10 test cards were delivered yesterday 4th Feb.
Now being evaluted.

Firmware:
Zipped versions of FPGA firmware sent to Emlyn end of last week.

BE/VME FPGA firmware. Concentrate design effort on Raw Data readout over VME.
Detailed report at FED-UK meeting today.

Test firmware based on ChipScope is evolving. Handing over responsibility for test firmware from FPGA designer to Test Engineer.

FED-PMCs:
50 bare PCBs have been received.
Expect all components to be in by end of March (lemo connectors currently longest lead.)
Assemble in April.
Test/Deliver in May-July.

Bug fixed (related to use of threads) in Module Test software. Perhaps explains inconsistent buffer effects observed when using multiple FEDs which was reported last year?