Project Monitor Form

Project: CMS FED **Date:** Wednesday 04 February-2004	**PMF number: 42** **Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

3 PMCs from USA repaired and shipped with 6 new PMCs on 30th January.
Expect to ship final batch of 6 to complete total of 40 next week.
Continue then to repair spares.
Update spreadsheets and status for next meeting.

FEDv1:

Manufacture

5 good PCBs (Ni/Au) arrived on 14th January as expected. (Drilling errors stopped all 7 being produced, 2 further good boards + 1 scrap board arrived following week).
Following visits to further assembly company the plans for assembly changed. Aim now to get experience with likely production manufacturer.

Quotes for assembly only were requested with CemGraft, STI and DDi.
Order with DDi passed to RAL procurement office on 2nd February.
Reasons for DDi: able to give guarantees on assembly (as they manufactured pcbs), use ODB++ for file transfer and were best price.

Assembly slot provisionally reserved for 2nd week in February.
Waiting for mechanical FPGA samples needed for thermal profiling tests.
Waiting for quotes for flying probe testing.
Discussing with DDi on passing list of modifications (e.g. new ADC termination resistors, do not fit list) in appropriate formats. FED is department's first job with DDi so a little learning curve.

Visited assembly company Cemgraft on 15th January.
Vistited assembly company DDi on 21st January.
Both companies had impressive manufacture, test and quality control facilities.

PCB production meeting with representatives from CMS and ATLAS held at RAL on 19th January. Minutes are available. Further meetings to be held monthly.
In general much better communications established between CMS and ATLAS on production issues.

Meeting with representatives from RAL Contracts on 23rd January to discuss refunds (possibly in kind) from manufacturer's of last FED production. Some more evidence from PCB company that boards made at a similar time to ours may have had problems with solder resist curing which could have caused solder bridges. It is planned to send one of bad FED boards to National Physical Laboratory for independent analysis.

FED Status:

Nr 005 is all ready for LSA tests. Expect to go to PISA after Tracker week (just waiting for CERN throttle card).

Second Fed nr 003 is now also under test at CERN. Occasional power up problems reported. No news yet if this was resolved. Otherwise operational.

Nr 002 was taken by Imperial after last meeting for S-LINK tests (see below).
Nr 006 and 007 were taken by Imperial after last meeting for power tests.

OptoRx removed and stored from Nr 008,009,010,011.

Future productions:
Xilinx FPGAs. Warning from distributor that lead times are getting very long (up to 15 weeks on some devices). Preparing details of costs of ordering parts for another N FEDs. Need to order soon to manufacture FEDv2 in summer.

System Tests

S-LINK tests based at Imperial (see talk at this meeting).
Using nr 002 and modified transition card given to Imperial after last meeting.
Working closely with Costas, Osman and James at Imperial good progress has been made.

First tests showed that data bits were swapped. Due to using slightly out of date schematics. Easily identified and fixed. Then saw identically formatted data transfer over S-LINK and VME. Learnt that FED-Kit also expects certain fixed values in DAQ header and trailer that weren't defined when Emlyn implemented code. Can be fixed. But these words can also be ignored. More sophisticated pattern generator firmware was requested and implemented.

S-LINK clock (80 MHz single ended) displays some kink structure probably due to termination on transition card. Should not have effect on correct data transfer, but can be cleaned up.
Good news is that no data transfer bit errors have been found to date.

Detailed readout tests at various trigger rates and event sizes are in progress.
Results are trying to be understood and correlated with buffer status bits and FED counters.
Trigger/readout rates seem to be limited. Don't think limit is the FED. If transition card is removed the FED can be driven at much higher rates.
Need to speed up system rates to do sensitive bit transfer tests.

FE FPGA algorithm tests at RAL:
PPD has shown that PROCESSED RAW DATA mode (ie re-ordering, pedestal subtraction and common-mode subtraction) in FE FPGA is working. Tests of ZERO SUPPRESSION MODE (ie cluster finding) are in progress. (see talk given at this meeting).
Note: the results of these tests are sensitive to correct adjustments of the adc sampling point via clock skews.

Firmware

Delay-FPGA:

Understood problems reported with setting clock skews. Due to different channel ordering convention in Delay FPGA compared to software. Meant that 1st and 3rd skews were correct but 2nd and 4th were swapped. Fixed in software.

After a bit of detective work the Spy Channel is also now working.
(Bug in Front-End logic had prevented serial data transfer on 2 out of 3 Delay chips)
Now observe Spy (pedestal data) from 4 channels on each Delay Chip. (Note Data starts after a fixed number of empty bits in serial stream). Successfully compared with normal readout data.
Channel ordering same as Clock Skew.
Note: Spy channel as implemented is triggered by software. We will probably need to modify to trigger on hardware to synchronise with frame capture.

FE-FPGA:

Bug for spy channel fixed (see above).
FIFO flags debugged with Bill Gannon.
Bill left RAL at end of January.

BE FPGA:

Improved pattern generator for S-LINK test implemented.

VME FPGA:

Serial interface to EPROM (for storage of ser nr etc) was completed and tested successfully.
Can read and write individual bytes to memory and protect selectable regions of memory.
Minor irritation is that we can set, but can’t read back control register.

Rate measurements of Block Transfer using SBS and HAL block transfer done in test crate with VMETRO Bus analyser module.
For 256 byte reads from FED event buffer average transfer = 2.4 microsecs => 1.6 Mbytes/sec
Compare with test on commercial memory card = 2.0 microsec => 2 Mbytes/sec
Neither very impressive. Indicates limiting factor is not the FED.
Nevertheless, more than an order of magnitude better than single reads with same interface.

Now have a fuller understanding of System ACE interface for in-situ reprogramming for FPGAs. Plan to keep firmware interface relatively simple and put most of work onto software.
Design specified and implementation just started.

ADM voltage monitor and LM82 serial interfaces still to implement. But should be straightforward copies of existing firmware blocks.

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Implement and start test of serial EPROM interface.	Done	ST, JC	
Debug Spy Channel logic.	Done	ST/EF/JC	
Update project pages for internal audit.	In progress	JC	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Update project pages for internal audit.	JC	27-02-04
Test access to System ACE registers.	ST/JC	27-02-04
Manage assembly and delivery of 6 more FEDs to RAL.	JC	01-03-04
Arrange to send bad FED to NPL	JC	15-02-04
Prepare order for further purchase of FPGAs	JC	06-02-04
Complete delivery of 40 PMCs to CERN	JC/JG	13-02-04

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 42**		
Project Manager: J. Coughlan **Date:** Wednesday 04 February-2004		**Sheet: 2 of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.5**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
17	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
18	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
20	New version OptoRx at RAL	01.04.03		21.07.03
21	FEDv1 Interim Review	08.09.03		11.09.03
22	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
23	Ship 1st FEDv1 to CERN.	30.09.03	31.10.03	03.11.03
24	Ship 2nd FEDv1 to CERN.	28.11.03	28.11.03	19.12.03
25	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		
26	Finalise design changes for FEDv2	01.04.04		
27	Design Review FEDv2	30.04.04		