Project Monitor Form

Project: CMS FED	**PMF number: 24**
Date: Tuesday 04-February-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

Status:

First pair of assembled FEDv1s (ser nr 001,002) arrived at RAL on 22nd January.
X-Rays of BGAs were done.
Full visual inspection was not carried out by Assembly company SAETech (they did inform us of this). In future we will wait for these inspections to be done.

Assembly issues:
Clamp diodes (x 192) had wrong pad footprint (our mistake). Needed rework by hand.
Will change part for future boards.
Some thru hole parts were done by us (e.g. TTC pin diode.)
Test connectors behind OptoRx not fitted (but may not be needed, see below.)
Bulk cap was too large for footprint. Done by hand.
No major issues up to board delivery.

Mechanical issues:
Front panels were fitted. Needed to insert/extract in crate.
Crate runners need to be 2.2 mm wide.
Board may need additional horizontal rigidity bars.
Nothing major.

Nb All tests so far on ser 001 only.
Collection of mods learnt from ser 001 will be applied to ser 002 before powering latter board.

Started with Power tests in VME crate.
(It proved difficult to power board reliably using bench supplies.)
Some patches needed to correctly sequence power on board.
Optimization of voltage windows on protection circuits needs to be done.
Power supply was only delivering 3.15V cf 3.3V (just needed pot adjustment.)
Intermittent power resets observed at first. Seem to have fixed this now.
Problem with missing core power to QDRs caused over heated chips (possibility of damage?)
Some LEDs didn't come on as expected (see below.)
Power was then on board for JTAG tests.

First JTAG tests. Carried out by lab JTAG expert and our designers.
BSDL files for BSCAN devices were ok. Devices recognised ok.
Files modified to bypass some non-BSCAN devices and drive all devices on chains appropriately.

Simplest connectivity tests of ~ 3K nets. Nb Further 3K nets not JTAGed.
Connections between FPGAs seemed ok.
Found 20 or so "errors" reported:
TTC (probably ok, floating inputs.)
QDRs (by driving chip enables appropriately these errors were removed.)

FPGA to ADCs (some shorts found, not all faults can be detected. Almost all solder bridges on resistor packs. After modifying board errors removed.)

Later more extensive JTAG soak tests (driving all combinations of i/os) carried out successfully. No errors so far.

Need VME Extender card to do "loop back" to rear connectors boundary scan which completes JTAG testing.

JTAG tools and testing process very impressive.

Summary of repairs (due to Assembly) so far.
Found (and fixed) several solder bridges on resistor packs between ADCs and Delay FPGAs. Nb very small devices/pins. (Nb Also fixed on ser 002.)
Some LEDs were found to be reversed.
Nb Full inspection by Assembly company may have avoided these repairs.

A list of problems is being kept and information will be passed back to SAETech.
We will also discuss with them later how best to reduce assembly costs whilst maintaining quality of manufacture.

Fitted 40 MHz local oscillator.

To test analogue front end circuitry need chip scope (embedded logic analyser) data capture in FPGA.

Next step:
Try to load FPGAs using Xilinx cables and JTAG chains.
36 Xilinx devices on a single chain.

When tests are more advanced on ser 001 we will start on ser 002.
Power issues on 001 can then be investigated more thoroughly.

18 off OptoRx from CERN were received at RAL by 28th Jan.

Electrical Test Card:
Cross-point switch pcbs quotes obtained. (20 0ff on panel).
We plan to use probe pins on the test card to fit directly into FED (removes need to connector on motherboard.)
Job hasn't gone out yet. Design was on hold awaiting final mods. Go for 5 day turnaround.

Firmware:
Test firmware slightly modified in light of early JTAG results.
Ready to be used for clock tests.

Meeting at RAL with Emlyn was held to show latest design and discuss modifications of event header code.
There is a problem with porting code between machines with new version of FPGA tools. Full pathnames in design files (including hard drive) seem to be required. We need a workaround.

FED-PMCs:
PMC nrs 31 (fitted with EPROM) and 32 (ser nr reloaded) sent from RAL on 3rd February.

Go ahead given for a further manufacture of 40 PMCs.
With no design changes.
All production and testing to be done at RAL.
50 off Xilinx XC4036XL ordered as last chance purchase.
Requisitions started. Propose to order other critical components and PCBs for 50 off.

PMC test set up has to move onto bench next to 9U FED area.

New cost code for PMC = FK70700
Effort code for PMC = FK50050