

Project Monitor Form

Project: CMS FED	PMF number: 07
Date: Monday 04-February-2002	Sheet: 1 of 2
<p>News and comment Feasibility Study continues.</p> <p><i>Front End Module:</i> Not much progress from DO to report due to work on other projects. Chris has been provided with full details of I/O to OptoRx. Improved OptoRx pin arrangement can be made once overview has been done.</p> <p><i>Firmware:</i> Request from customer for a new requirement on FE FPGA to handle reversed polarity signals.</p> <p><i>Board level:</i> Saeed is working on an overview of power supplies to board.</p> <p><i>Other issues:</i> As a guide to potential savings for CMS final production, Bob T. obtained an estimate for production of 500 H1 FTT boards at £300 (cf £700 for 30 off). ADC 65MHz quote was obtained. Lead time of 2-3 weeks. We will go ahead with ordering 500 for 10 FF1s. However, spend on FPGAs this FY is not possible. Orders can only be taken starting in March. Lead time is then 10-12 weeks.</p>	

Actions from the previous PMF			
Action	Status	Who	Target date
Pass component details for purchases this FY to Bob T.	Done	JC	
Investigate tools to create CADENCE symbols of Xilinx FPGA.	Ongoing	RH	21-01-02
Test key aspects of Delay FPGA on development board in Lab	In progress	EF/RH	31-02-02
Produce preliminary pinout of Delay FPGA.	In progress	EF	11-02-02
Obtain estimate for PCB manufacture 500 H1FTT as guide of CMS costs.	On going	CD	18-02-02
Obtain estimate for assembly 500 H1FTT as guide of CMS costs.	Done	BT	18-02-02
Specify board level voltage and current requirements.	In progress	ST	18-02-02
Book cards 9U FED into Drawing Office	Done	AB	

Request Nicky to add members to cmsfed unix group for web access.	Done	JC	
Produce proposal for web pages reorganisation	On going	AB	04-02-02

Actions outstanding and new actions		
Action	Who	Target Date
Investigate tools to create CADENCE symbols of Xilinx FPGA.	RH	11-02-02
Test key aspects of Delay FPGA on development board in Lab	EF/RH	31-02-02
Produce preliminary pinout of Delay FPGA.	EF	11-02-02
Obtain estimate for PCB manufacture 500 H1FTT as guide of CMS costs.	CD	18-02-02
Investigate temperature monitoring of FE Module (OptoRx/ Virtex)	JS	28-02-02
Specify board level voltage and current requirements.	ST	18-02-02
Ask R. Stephenson if we can borrow simulations tools license for James's PC.	RH	11-02-02

Project Monitor Form- milestones

Project: CMS FED		PMF number: 07		
Project Manager: R. Halsall		Sheet: 2 of 2		
Date: Monday 04-February-2002				
	Milestones from Project Management Plan Version:	date due in PMP	predicted date	date done
1	User Requirements Document	30-07-01		26-09-01
2	Project Spec sign off	21-12-01	31-01-02	
3	Board Level Preliminary Review	14-01-02		16-01-02
4	FE Analogue Channel Feasibility Review	31-01-02	31-01-02	
5	FE Module Feasibility Review	28-02-02	28-02-02	
7	Board Level Feasibility Review	04-03-02	04-03-02	
8	Delay FPGA Feasibility Review	31-01-02	31-01-02	
9	Front End FPGA Feasibility Review	31-01-02	31-01-02	
10	Back End FPGA Feasibility Review	31-01-02	31-01-02	
11	VME FPGA Feasibility Review	28-02-02	28-02-02	
12	Clock FPGA Feasibility Review	28-02-02	28-02-02	
13	Release Test Plan Document	22-02-02	22-02-02	