Project Monitor Form

Project: CMS FED	**PMF number: 40**
Date: Wednesday 03 December-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

FED-PMCs:

Jonathan Godwin came back to RAL this week and is re-starting PMC repair work
3 remaining PMCs from USA will be returned soon for resistor repair.

FEDv1:

Manufacture

Repair on boards has been less successful than hoped.
Poor quality of pcbs makes rework difficult.

Inspection at RAL using "Ersascope" like tool (on loan) shows several problems remaining under BGAs.

Proposal for 6 boards:

06. Return to Assembly to replace 2 Delay FPGAs.
07. Check TTCrx error.
08. Stop repair work. Recover OptoRx.
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10. Stop repair work. Recover OptoRx.
11. Try replacing one FE FPGA using Imperial BGA rework kit?

Would not recommend using repaired boards outside UK.

Re-balling of just XCV2000 FPGAs is going ahead (cost is £35 each).

Better news from our sister project…
2 assembled CALICE boards came back last week (Immersion Tin.)
Both boards passed BScan tests. Only minor mods necessary.
Board quality is judged very high standard.
Power circuits incorporating proposed changes to FEDv2 worked with only one minor mod.
Tests are continuing.

Visited assembly companies STI (25.11) and SAETech (02.12)

System Tests

RAL LHC crate equipped with 6U kit.
New crate is being set up with second SBS cards as second rig at RAL for software tests.
(odd behaviour accessing FED registers observed with SBS controller as arbiter but not in slot 1)

Current measurement (with just FED 002 in crate):
+3.3V : 13A
+5V: 4A (only 4 OptoRx on board)
+12V : 0.6A
-12V : 0 A
Power : 70 W
Measurements in agreement with earlier ones from James.
Needs to be re-measured with all OptoRx and driving inputs.

Firmware

Good progress has been made in identifying and fixing bugs reported from system tests at CERN and software tests at RAL.

Update of firmware set released to Imperial and CERN on 02.12 (see details below.)
Delay 02_19; FE 03_0D; BE 02_2C; VME 03_04

Important to keep compatible versions of BE and VME designs.
Need to re-check CERN and UK readout results with updated firmware.

Delay-FPGA:

To do: Test Spy Channel. Minor changes needed in VME serial for this.

FE-FPGA:

Two reported bugs were quickly identified and fixed by Bill Gannon
a) pedestal loading logics, b) apv data of every 256th event misssing.
After fix found new bit file did not distribute clocks to 3rd Delay FPGA in each group.
Eventually problem localised to tools installation on Saeed's PC. Not understood and tools expert away. Rebuild on another machine and problem disappears.

Software tests of Processed Raw Data and Zero Suppressed modes using OptoTester pattern input have started.

Saeed is about to implement code to increase FE buffer depths for raw data readout.

BE FPGA:

Bug reported in readout from system tests was found in simulation and fixed. Problem had caused events to be stuck in QDR if more than one event was stored at a time.

Minor change is needed to Emlyn's DAQ header block to get VME and S-LINK event formats to match exactly.

Logic for S-LINK is implemented.
Transition card has been modified to match S-LINK signals.
Ready to start tests with FEDKits.
One mod will be needed on FED to deliver power to Transition card.

VME FPGA:

To do: System ACE interface and EPROM interface.
Mods for testing spy channel needed.

Bug still exists which causes readout inconsistencies for events larger than 2 event buffers (i.e. > 64 Kbytes). Therefore problem doesn't affect normal size events.

Clock re-setting and error recovery are being improved.