

Project Monitor Form

Project: CMS FED	PMF number: 40
Date: Wednesday 03 December-2003	Sheet: 1 of 2

Project Implementation phase.

FED-PMCs:

Jonathan Godwin came back to RAL this week and is re-starting PMC repair work
3 remaining PMCs from USA will be returned soon for resistor repair.

FEDv1:

Manufacture

Repair on boards has been less successful than hoped.
Poor quality of pcbs makes rework difficult.

Inspection at RAL using “Ersascope” like tool (on loan) shows several problems remaining under BGAs.

Proposal for 6 boards:

06. Return to Assembly to replace 2 Delay FPGAs.
07. Check TTCrx error.
08. Stop repair work. Recover OptoRx.
09. Stop repair work. Recover OptoRx.
10. Stop repair work. Recover OptoRx.
11. Try replacing one FE FPGA using Imperial BGA rework kit?

Would not recommend using repaired boards outside UK.

Re-balling of just XCV2000 FPGAs is going ahead (cost is £35 each).

Better news from our sister project...
2 assembled CALICE boards came back last week (Immersion Tin.)
Both boards passed BScan tests. Only minor mods necessary.
Board quality is judged very high standard.
Power circuits incorporating proposed changes to FEDv2 worked with only one minor mod.
Tests are continuing.

Visited assembly companies STI (25.11) and SAETech (02.12)

System Tests

RAL LHC crate equipped with 6U kit.
New crate is being set up with second SBS cards as second rig at RAL for software tests.
(odd behaviour accessing FED registers observed with SBS controller as arbiter but not in slot 1)

Current measurement (with just FED 002 in crate):

+3.3V : 13A

+5V: 4A (only 4 OptoRx on board)

+12V : 0.6A

-12V : 0 A

Power : 70 W

Measurements in agreement with earlier ones from James.

Needs to be re-measured with all OptoRx and driving inputs.

Firmware

Good progress has been made in identifying and fixing bugs reported from system tests at CERN and software tests at RAL.

Update of firmware set released to Imperial and CERN on 02.12 (see details below.)

Delay 02_19; FE 03_0D; BE 02_2C; VME 03_04

Important to keep compatible versions of BE and VME designs.

Need to re-check CERN and UK readout results with updated firmware.

Delay-FPGA:

To do: Test Spy Channel. Minor changes needed in VME serial for this.

FE-FPGA:

Two reported bugs were quickly identified and fixed by Bill Gannon

a) pedestal loading logics, b) apv data of every 256th event missing.

After fix found new bit file did not distribute clocks to 3rd Delay FPGA in each group.

Eventually problem localised to tools installation on Saeed's PC. Not understood and tools expert away. Rebuild on another machine and problem disappears.

Software tests of Processed Raw Data and Zero Suppressed modes using OptoTester pattern input have started.

Saeed is about to implement code to increase FE buffer depths for raw data readout.

BE FPGA:

Bug reported in readout from system tests was found in simulation and fixed. Problem had caused events to be stuck in QDR if more than one event was stored at a time.

Minor change is needed to Emlyn's DAQ header block to get VME and S-LINK event formats to match exactly.

Logic for S-LINK is implemented.

Transition card has been modified to match S-LINK signals.

Ready to start tests with FEDKits.

One mod will be needed on FED to deliver power to Transition card.

VME FPGA:

To do: System ACE interface and EPROM interface.
Mods for testing spy channel needed.

Bug still exists which causes readout inconsistencies for events larger than 2 event buffers (i.e. > 64 Kbytes). Therefore problem doesn't affect normal size events.

Clock re-setting and error recovery are being improved.

Actions from the previous PMF			
Action	Status	Who	Original Target date
Complete S-LINK firmware.	Done	ST	
Modify S-LINK transition card.	Done	ST	
Commission LHC crates.	Done	IC	

Actions outstanding and new actions		
Action	Who	Target Date
Fix clock resetting logic.	ST	12-12-03
Deepen FE buffers.	ST	12-12-03
Produce summary of status of 6 "Tin" FEDs.	IC	08-12-03
Fit OptoRx modules to 002 and 004.	IC	12-12-03

Project Monitor Form- milestones

Project: CMS FED		PMF number: 40		
Project Manager: J. Coughlan				
Date: Wednesday 03-December-2003		Sheet: 2 of 2		
	Milestones from Project Management Plan Version:1.5	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off & PCB Tape Out	07.10.02		06.12.02
17	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
18	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
20	New version OptoRx at RAL	01.04.03		21.07.03
21	FEDv1 Interim Review	08.09.03		11.09.03
22	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
23	Ship 1st FEDv1 to CERN.	30.09.03	31.10.03	
24	Ship 2nd FEDv1 to CERN.	28.11.03	28.11.03	