Project Monitor Form

Project: CMS FED	**PMF number: 28**
Date: Wednesday 02-April-2003	**Sheet:** 1 **of** 2

Project Implementation phase.

Status:
Tests still proceeding to schedule.

Opto Testing
Matt assisting with Opto and VME tests at RAL.
Laser safety requirements implemented to use Opto Test card.

Ser 001 came back Wed 19th with 2 x OptoRx and replaced QDRs.
Agreed to do one weeks opto testing at RAL to familiarise with tools …etc.
JTAG tests repeated. Ok.
Power on 001 ok.
Chip Scope on 001 saw pedestal levels after setting OptoRx contol lines. Noise level not noticeably worse with OptoRx.
Plugged in Opto Test card inputs…but…

Observed odd problem with loading from Cflash on ser 001 at power on. Loading of FPGAs appeared to complete and then immediately all FPGAs unloaded.
Not seen on ser 002. Not seen on either when loading via parallel cable.
Problem started when changing Cflash card contents.
Reconstructed old card contents and 001 loaded again.
Narrowed down to driving OptoRx control lines in new version.
Eventually understood as due to power 3.3V line trip. See spike in 3.3 current. Power recovers automatically, but FPGA load isn't retried.
Nb OptoRx only use 5V. Some dependency between 3.3and 5V. Problem only manifests at power on.
Fixed by relaxing trip level on FET controller.
LEDs on FPGAs and System ACE very useful in debugging.

First Opto Test card inputs recorded by Chip Scope successfully.
Ramps, square waves, APV frame like data (will be ideal for header testing.)

FED ser001 and OptoTest card went to Imperial on Wednesday 12th as planned.
With cross-point test card and existing test firmware.

Tests at RAL continue with ser 002.

Firmware
Delay FPGA: Final design loaded.
Double Data rate to FE FPGA worked after adjusting clock skew.

BE FPGA: Implementing data path and control from QDR to VME.
DAQ header block now included.

FE-FPGA: work started on getting final design loaded.

VME-FPGA: see below. Serial comms block ready to test.

VME Tests

Matt installed NI/VXI interface to Linux PC in FED crate.
Simple software example for VME access under HAL.
Single cycle reads and writes tested.

New version of VME firmware with fix for Block Transfer installed.
Tested with NI/VXI. Block transfer tests passed. Later repeated with RIO.
Need to check change in mirrored memory windows.

Protocol (based on polling) for FED(BE/VME)-CPU for VME readout defined.
Offsets in VME for major register blocks defined.

FED-PMCs:
First 10 assembled PMCs expected this week at RAL. Ahead of schedule.
Then expect 10 more next 3 weeks.
Test effort requested. Need to set up test bench.
FEDv1 NI/VXI cards borrowed from PMC test bench. SBS interface for FEDv1?