

Project Monitor Form

Project: CMS FED	PMF number: 28
Date: Wednesday 02-April-2003	Sheet: 1 of 2

Project Implementation phase.

Status:
Tests still proceeding to schedule.

Opto Testing
Matt assisting with Opto and VME tests at RAL.
Laser safety requirements implemented to use Opto Test card.

Ser 001 came back Wed 19th with 2 x OptoRx and replaced QDRs.
Agreed to do one weeks opto testing at RAL to familiarise with tools ...etc.
JTAG tests repeated. Ok.
Power on 001 ok.
Chip Scope on 001 saw pedestal levels after setting OptoRx control lines. Noise level not noticeably worse with OptoRx.
Plugged in Opto Test card inputs...but...

Observed odd problem with loading from Cflash on ser 001 at power on. Loading of FPGAs appeared to complete and then immediately all FPGAs unloaded.
Not seen on ser 002. Not seen on either when loading via parallel cable.
Problem started when changing Cflash card contents.
Reconstructed old card contents and 001 loaded again.
Narrowed down to driving OptoRx control lines in new version.
Eventually understood as due to power 3.3V line trip. See spike in 3.3 current. Power recovers automatically, but FPGA load isn't retried.
Nb OptoRx only use 5V. Some dependency between 3.3and 5V. Problem only manifests at power on.
Fixed by relaxing trip level on FET controller.
LEDs on FPGAs and System ACE very useful in debugging.

First Opto Test card inputs recorded by Chip Scope successfully.
Ramps, square waves, APV frame like data (will be ideal for header testing.)

FED ser001 and OptoTest card went to Imperial on Wednesday 12th as planned.
With cross-point test card and existing test firmware.

Tests at RAL continue with ser 002.

Firmware
Delay FPGA: Final design loaded.
Double Data rate to FE FPGA worked after adjusting clock skew.

BE FPGA: Implementing data path and control from QDR to VME.
DAQ header block now included.

FE-FPGA: work started on getting final design loaded.

VME-FPGA: see below. Serial comms block ready to test.

VME Tests

Matt installed NI/VXI interface to Linux PC in FED crate.
Simple software example for VME access under HAL.
Single cycle reads and writes tested.

New version of VME firmware with fix for Block Transfer installed.
Tested with NI/VXI. Block transfer tests passed. Later repeated with RIO.
Need to check change in mirrored memory windows.

Protocol (based on polling) for FED(BE/VME)-CPU for VME readout defined.
Offsets in VME for major register blocks defined.

FED-PMCs:

First 10 assembled PMCs expected this week at RAL. Ahead of schedule.
Then expect 10 more next 3 weeks.
Test effort requested. Need to set up test bench.
FEDv1 NI/VXI cards borrowed from PMC test bench. SBS interface for FEDv1?

Actions from the previous PMF			
Action	Status	Who	Original Target date
Produce FED software driver lib API.		JC	29-11-02
Run with Delay FPGA design in FED.	Done	IC/EF	
Deliver FED with 2 OptoRx to IC.	Done	JC/MN	
Get OptoTest card bench working at RAL.	Done	MN	
Debug block transfer VME FPGA.	Done	EF/JC/MN	
Test serial comms between VME and BE FPGA.		EF/JC	28-03-03
Test FE to BE FPGA and QDR data write path.	Done	IC/ST	04-04-03

Actions outstanding and new actions		
Action	Who	Target Date
Produce FED software driver lib API.	JC	17-04-03
Get OptoTest card bench working at RAL.	MN	21-03-03
Test serial comms between VME and BE FPGA.	EF/JC	04-04-03
Test FE to BE FPGA and QDR data write path.	IC/ST	17-04-03

Project Monitor Form- milestones

Project: CMS FED		PMF number: 28		
Project Manager: J. Coughlan				
Date: Wednesday 02-April-2003		Sheet: 2 of 2		
	Milestones from Project Management Plan Version:1.3	date due in PMP	predicted date	date done
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
7	Board Level Feasibility Review	25.02.02		25.02.02
8	Delay FPGA Interim Review	11.03.02		27.03.02
9	Front End FPGA Interim Review	28.02.02		12.08.02
10	Back End FPGA Interim Review	04.03.02		17.12.02
11	FE Module Final Review	18.06.02		25.06.02
12	BE Module Interim Review	28.06.02		15.08.02
13	Schematics finalised	05.08.02		22.08.02
14	Layout & Routing done	16.09.02		29.12.02
15	Full Board Design Final Review	23.09.02		06.11.02
16	IDR Customer Production sign off & PCB Tape Out	07.10.02		06.12.02
17	Batch 0 (2 off) Non-Opto Assembled boards at RAL	11.11.02		22.01.03
18	OptoRx for Batch 0 in UK	26.08.02		28.01.03
19	Batch 0 review	11.04.03		
20	OptoRx for Batch 1 at RAL	01.04.03		
21	Batch 1 (10 off) Assembled boards at RAL	04.07.03		
22	Delivery Batch 1 to CERN start	12.09.03		
23	Delivery Batch 1 to CERN completed.	04.12.03		