Project Monitor Form

Project: CMS FED **Date:** Friday 10 Oct-2004	**PMF number: 50** **Sheet:** 1 **of** 2

Project Implementation phase.

FEDv2

First 2 FEDv2 boards (ser nr 18 & 19) passing all VME based readout tests.
(LabView analogue tests done, but couldn't be repeated at RAL this week).
Air deflector bars fitted. Bar code fitted.
(NB JTAG for re-programming VME FPGA is now on J0 connector).
Temp sensor I2C readout errors appear to be spurious as the readings are correct (Firmware bug yet to be understood)

Board nr 18 brought to Imperial today for tests with Transition card.

Next batch of 20:

Provisional quotes for PCB and Assembly of 20,25 and 30 off obtained.

Elantec 2104C differential amplifier in Front Ends (96 per board) are on last time buy. Order for production quantities is being placed. We also need a few more to complete kit for next 20 off, but not on critical path.
Still waiting for QDRs.

FEDv1:

FEDv1 ser nr 17 brought to Imperial on 23 Sept for S-LINK merging tests (to replace ser nr 002).
Locations of all boards are on summary spreadsheet linked to usual Fed web pages.
www.te.rl.ac.uk/esdg/cms-fed/qa_web

Testing :

Mark Raymond modified ser nr 002 with various values of Rload and Caps as agreed for settling time tests (see his note). Board is now with Francois's group. RAL engineers will be at CERN next week to aid with tests if necessary.

S-LINK tests at high rates and large events show various and intermittent problems.
CRC checksum errors, event length mismatches etc
Dumps of bad events are being collated and sent to RAL.

Firmware :

All 4 FPGA designs have been migrated to latest release of FPGA design/Xilinx tools (new

synthesis tools).

Implementation of List of Missing Features in URD has started.

Delay FPGA firmware version can now be read back (need corresponding software).

TTC chan B commands in progress.
Behaviour on overflow of data and trigger buffers.
Error monitoring registers.

Other Items

The small pcb which is used to distribute the JTAG programming line along J0 connector is now in manufacture (5 off). We will need 2 FEDv2s to test this.

Ivan has found a patch which cures problems observed when reformatting Compact Flash cards using some Windows XP machines (see note on web).

RAL engineers at CERN next Tuesday and Wednesday during 25 nsec beam test.

FEDs in beam test upgraded to latest standard release.

ACE File: 16_07_04_1500 = (Delay 02_1B ; FE 03_16 ; BE 02_43)
EPROM : VME_03_0F

NB after beam test:
Must upgrade boards at CERN (to be FEDv2 compatible) by simple addition of couple of LVDS clock resistors.

Tender :

Invitation to Tender document (with FED as one of quotes) was sent out on 13th September. The return date is 27th October.
The details of the criteria for company selection and membership of panel are yet to be finalised. The aim is to complete the evaluation in November (although there is no formal time limit on this step).

Actions from the previous PMF			
Action	**Status**	**Who**	**Original Target date**
Draft of LECC paper on FED Manufacture		JC	Done
Prioritize Firmware tasks for 2004.		JC/ST	Done
Verify design of FEDv2.		IC/JC	29-10-04
Testing Specification document for Assembly company	Draft done	IC	06-09-04
Port FPGA code to new tools.	Done	ST	

Actions outstanding and new actions		
Action	**Who**	**Target Date**
Testing Specification document for Assembly company.	IC	06-09-04
Verify design of FEDv2.	IC/JC	29-10-04
Implement Firmware for TTC chan B commands	ST	06-12-04

Project Monitor Form- milestones

Project: CMS FED		**PMF number: 50**		
Project Manager: J. Coughlan **Date:** Friday 10 Oct-2004		**Sheet: 2** **of** 2		
	Milestones from **P**roject **M**anagement **P**lan Version**:1.6**	**date due in PMP**	**predicted date**	**date done**
1	User Requirements Document	30.07.01		26.09.01
2	Project Spec sign off	21.12.01		05.02.02
3	Board Level Preliminary Review	14.01.02		16.01.02
4	FE Analogue Channel Feasibility Review	31.01.02		21.03.02
5	FE Module Feasibility Review	28.02.02		08.05.02
6	Board Level Feasibility Review	25.02.02		25.02.02
7	Delay FPGA Interim Review	11.03.02		27.03.02
8	Front End FPGA Interim Review	28.02.02		12.08.02
9	Back End FPGA Interim Review	04.03.02		17.12.02
10	FE Module Final Review	18.06.02		25.06.02
11	BE Module Interim Review	28.06.02		15.08.02
12	Schematics finalised	05.08.02		22.08.02
13	Layout & Routing done	16.09.02		29.10.02
14	Full Board FEDv1 Design Final Review	23.09.02		06.11.02
15	IDR Customer Production sign off &PCB Tape Out	07.10.02		06.12.02
16	Batch 1 (2 off) Non-Opto Assembled FEDv1s at RAL	11.11.02		22.01.03
17	Old version OptoRx for Batch 0 in UK	26.08.02		28.01.03
18	Batch 2 (3 off incl 1 Opto) Assembled boards at RAL	20.06.03		27.06.03
19	New version OptoRx at RAL	01.04.03		21.07.03
20	FEDv1 Interim Review	08.09.03		11.09.03
21	Batch 3 (6 off all opto) Assembled boards at RAL	30.09.03		08.10.03
22	Ship 1st FEDv1 to CERN.	30.09.03		03.11.03
23	Ship 2nd FEDv1 to CERN.	28.11.03		19.12.03
24	Batch 4 (6 off DDi) Assembled boards at RAL	01.03.04		22.03.04
25	Finalise design changes for FEDv2	01.04.04		25.03.04
26	Design Review FEDv2	18.06.04		04.06.04
27	FEDv2 tape-out	16.07.04		28.06.04
28	First FEDv2 boards at RAL	08.10.04		02.08.04
29	Dispatch calls for Tender	26.08.04		13.09.04
30	Award Tender contract	09.02.05		
31	FEDv3 tape-out	06.04.05		
32	First FEDv3 boards at RAL	13.07.05		
33	Production of 500 FEDv3 starts	08.09.05		
34	First FEDv3 at B904 Prevessin	30.11.05		
35	First FED installed at USC55	17.11.05		
36	Last FED installed at USC55	26.07.06		
37	Power on Tracker	01.08.06		
38	Readout test with Tracker	01.10.06		
39	LHC test run	02.04.07		