FED Status

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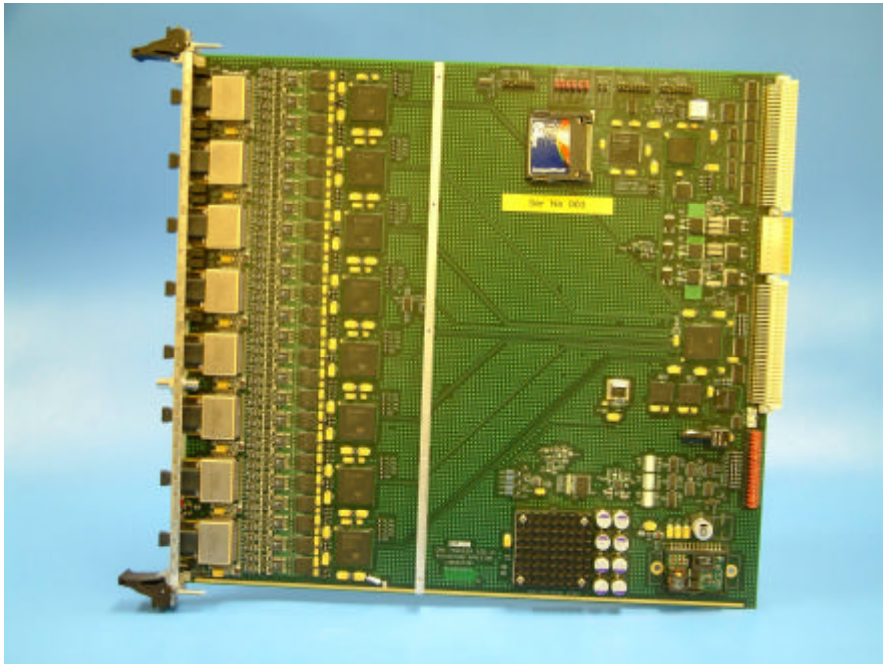
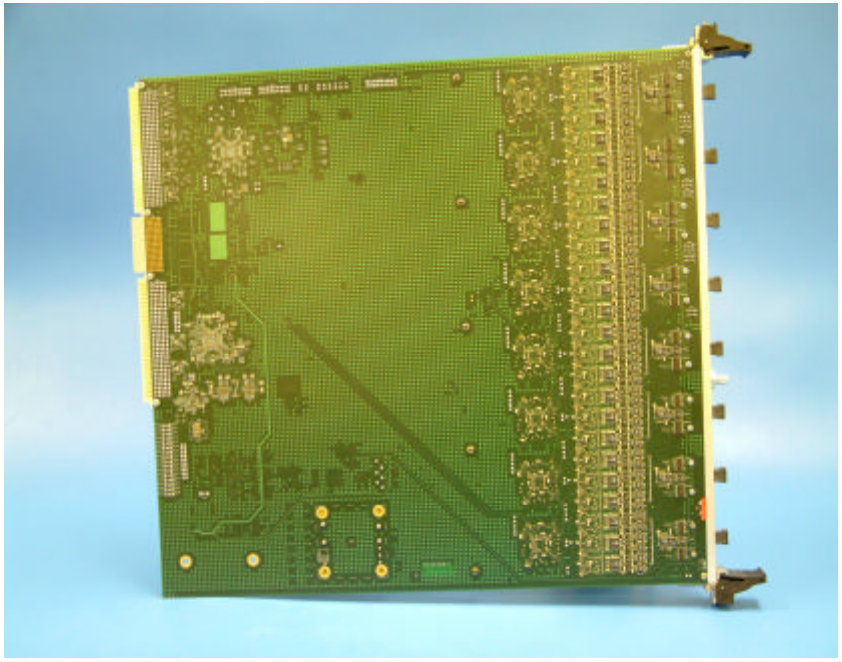
presented by John Coughlan RAL

FEDv1 Summary





17 FEDv1 boards manufactured (11 working). No more to be made.

6 commissioned at RAL and delivered to CERN for LSA (4 used in Beam Tests)

5 working boards kept for design testing. (could release 2 of these if needed).

FEDv1 Design Testing

- Objectives
  - Validate final design — done
  - Production manufacture acceptance tests — well advanced
- Hardware — *few issues studied and resolved during testing*

  Verified @ 100 kHz L1 S-LINK readout @ 80 MHz. TTC and TCS Interfaces verified

  Analogue performance excellent. Optical inputs using FED Opto-Tester board.

  To optimise OptoRx (1% settling in 15ns) some FE component values need final tuning. A board has been modified with several different component values. Tests to be completed at CERN after beam tests (see talk by Stefanos).

  Power/temp requirements finalised. Standard LHC crates satisfactory.
- Firmware — *complete and working for assembly test use*

  Used in 25 nsec Test Beams June 2004.

  Few minor issues (as expected!) under investigation.
- Software — *fully integrated in CMS Tracker DAQ framework.*

  Test bench Framework for essential Assembly Plant Testing nearly ready

FEDv2 pre-Production Board

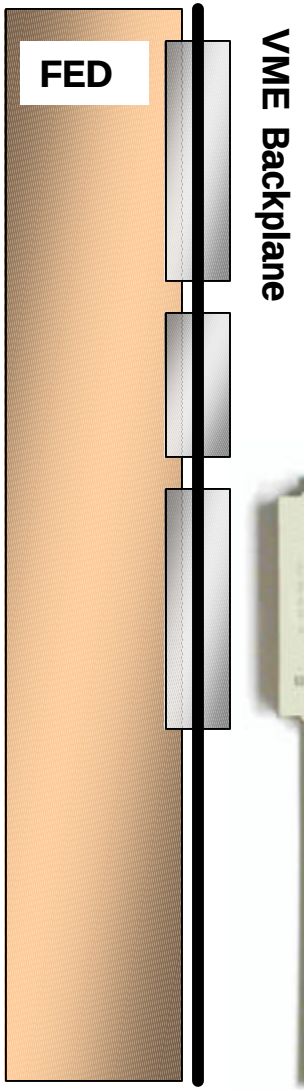
- Aim to be final production version - minimal changes from v1
  - Power Block : General improvements.
  - QDR Memory : Replacement part (pin compatible) identified and on order.
  - FE FPGA : Use larger 2M gate (pin compatible) part.
  - ADC : AD9218 Device bug. Reduce gain by half. Simple mod.
  - FPGA Configuration : Boot device reprogram via VME J0 / JTAG cable.
  - S-LINK & TCS Signals : New 6U VME Transition Card.
  - FE Analogue : Tune few components for optimal matching to Optical Link

- Status

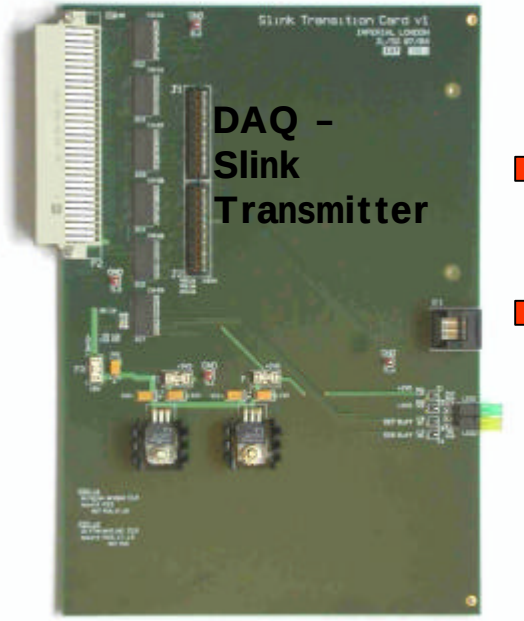
  First 2 boards received in August as scheduled. Tests proceeding well.
  Boundary Scan passed. VME based readout tests working.
  S-LINK tests in progress with new Transition card.

- Plan to make a further ~20 at end of 2004 for Full Crate tests.

S-LINK Transition Card



- Carrier for slink transmitter
  - 6U VME Transition card
  - 1 per FED
  - Buffers control and data signals
  - Buffers throttle signals
  - FED v1 and V2 compatible
- Status
  - 3 returned from manufacture in August.
  - Under tests with FEDs

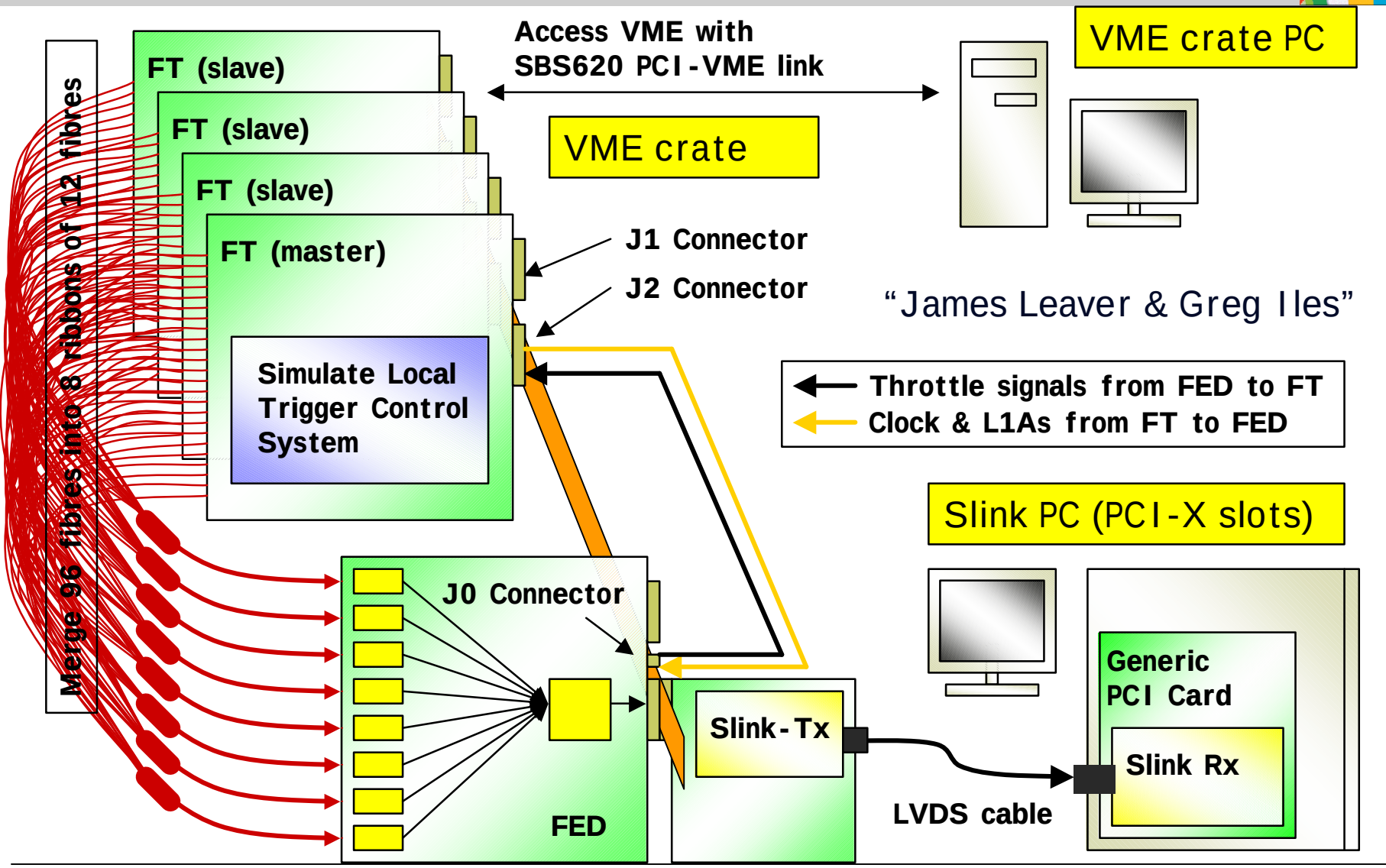


Slink data and control signals

Throttle signals to FMM

James Leaver

S-LINK Test setup



S-LINK Tests

- Test conditions
  - Trigger rate = 100 kHz “fixed” ; Known pattern data sent from FED
  - Level of checking is rate dependent , limited by receiver in PC
  - Some time spent understanding how S-LINK DAQ card operates. Eg CRC checking
- Test results
  - Errors observed with FEDv2 (stuck bits), problems not seen with FEDv1 board.
  - Verified transition card design is OK.
  - Suspected problems with FEDv2 pcb/layout?
  - Now almost certain this is a rather subtle firmware problem caused by use of new FPGA design tools.
  - Now testing with 100 kHz random triggers and Zero Suppressed data.

Validation Testing at Assembly Plant

0. Quality Controls during Assembly process
AOI, X-ray

1. Custom Tests at Assembly Plant
BScan, VME crate

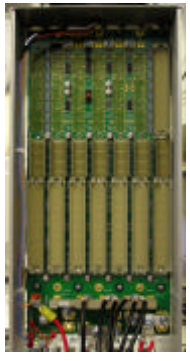
2. Tests at RAL & IC
OptoRx, Full crate

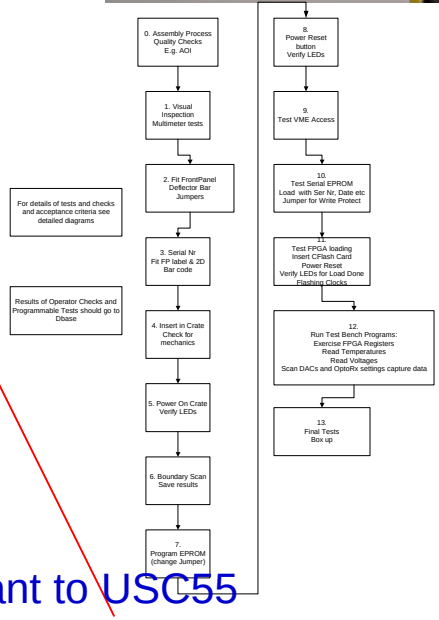
3. Tests at CERN
Prevessin 904
Readout Integration

4. Installation at CMS
USC55

Testing by Assembly plant operatives

Boundary Scan Testing for Digital



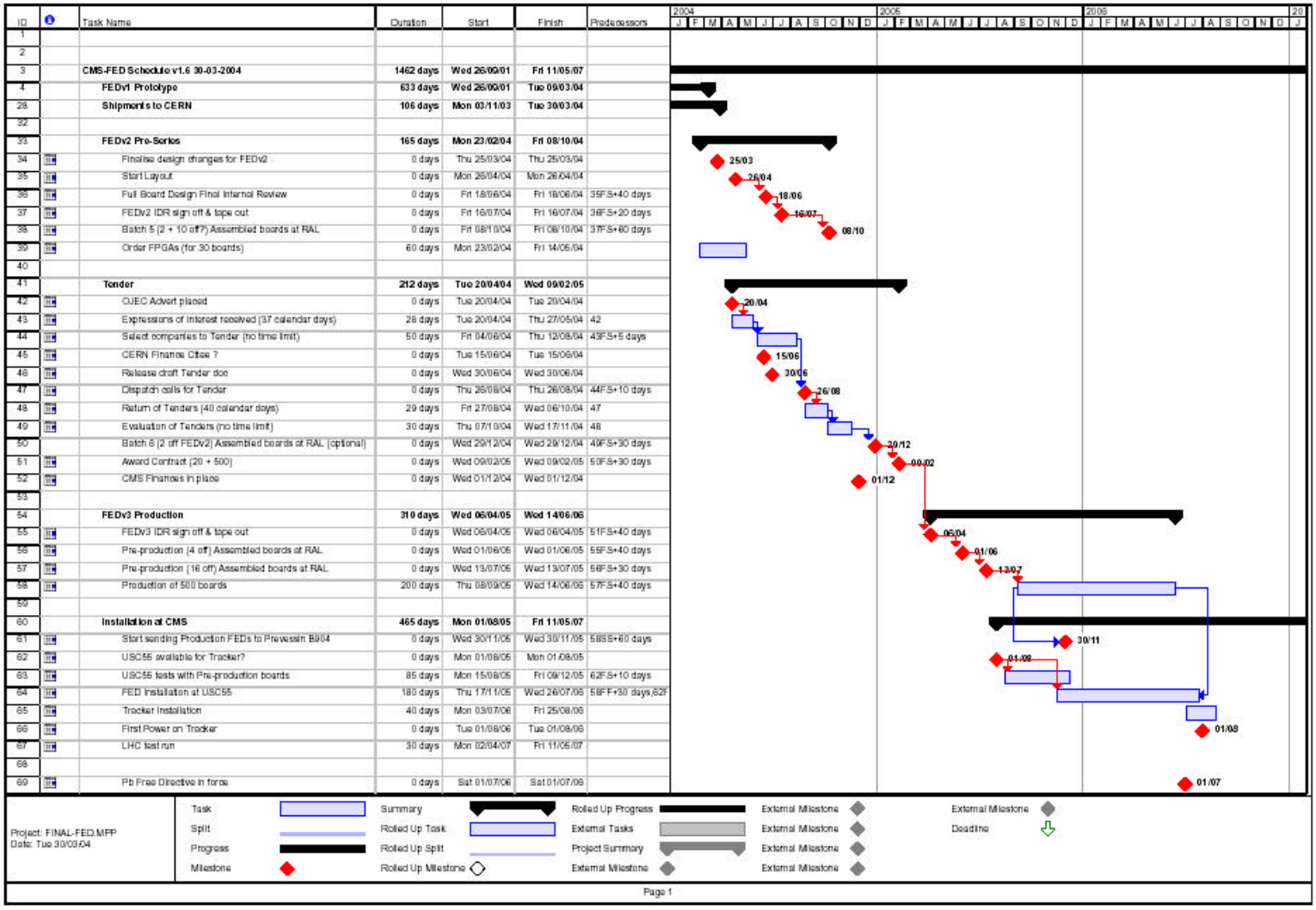


VME Crate Testing for Analogue

Test Flow from Assembly Plant to USC55

500 boards to test over 10 months. Essential to catch any manufacturing faults early.

FED Schedule v1.6 March 2004



ID	Task Name	Duration	Start	Finish	Predecessors
3	**CMS-FED Schedule v1.6 30-03-2004**	**1462 days**	**Wed 26/09/01**	**Fri 11/05/07**	
4	**FEDv1 Prototype**	**633 days**	**Wed 26/09/01**	**Tue 09/03/04**	
28	**Shipments to CERN**	**106 days**	**Mon 03/11/03**	**Tue 30/03/04**	
33	**FEDv2 Pre-Series**	**165 days**	**Mon 23/02/04**	**Fri 08/10/04**	
34	Finalise design changes for FEDv2	0 days	Thu 25/03/04	Thu 25/03/04	
35	Start Layout	0 days	Mon 26/04/04	Mon 26/04/04	
36	Full Board Design Final Internal Review	0 days	Fri 18/06/04	Fri 18/06/04	35FS+40 days
37	FEDv2 IDR sign off & tape out	0 days	Fri 16/07/04	Fri 16/07/04	36FS+20 days
38	Batch 5 (2 + 10 off?) Assembled boards at RAL	0 days	Fri 08/10/04	Fri 08/10/04	37FS+60 days
39	Order FPGAs (for 30 boards)	60 days	Mon 23/02/04	Fri 14/05/04	
40					
41	**Tender**	**212 days**	**Tue 20/04/04**	**Wed 09/02/05**	
42	OJEC Advert placed	0 days	Tue 20/04/04	Tue 20/04/04	
43	Expressions of Interest received (37 calendar days)	28 days	Tue 20/04/04	Thu 27/05/04	42
44	Select companies to Tender (no time limit)	50 days	Fri 04/06/04	Thu 12/08/04	43FS+5 days
45	CERN Finance Cttee ?	0 days	Tue 15/06/04	Tue 15/06/04	
46	Release draft Tender doc	0 days	Wed 30/06/04	Wed 30/06/04	
47	Dispatch calls for Tender	0 days	Thu 26/08/04	Thu 26/08/04	44FS+10 days
48	Return of Tenders (40 calendar days)	29 days	Fri 27/08/04	Wed 06/10/04	47
49	Evaluation of Tenders (no time limit)	30 days	Thu 07/10/04	Wed 17/11/04	48
50	Batch 6 (2 off FEDv2) Assembled boards at RAL (optional)	0 days	Wed 29/12/04	Wed 29/12/04	49FS+30 days
51	Award Contract (20 + 500)	0 days	Wed 09/02/05	Wed 09/02/05	50FS+30 days
52	CMS Finances in place	0 days	Wed 01/12/04	Wed 01/12/04	
53					
54	**FEDv3 Production**	**310 days**	**Wed 06/04/05**	**Wed 14/06/06**	
55	FEDv3 IDR sign off & tape out	0 days	Wed 06/04/05	Wed 06/04/05	51FS+40 days
56	Pre-production (4 off) Assembled boards at RAL	0 days	Wed 01/06/05	Wed 01/06/05	55FS+40 days
57	Pre-production (16 off) Assembled boards at RAL	0 days	Wed 13/07/05	Wed 13/07/05	56FS+30 days
58	Production of 500 boards	200 days	Thu 08/09/05	Wed 14/06/06	57FS+40 days
59					
60	**Installation at CMS**	**465 days**	**Mon 01/08/05**	**Fri 11/05/07**	
61	Start sending Production FEDs to Prevessin B904	0 days	Wed 30/11/05	Wed 30/11/05	58SS+80 days
62	USC55 available for Tracker?	0 days	Mon 01/08/05	Mon 01/08/05	
63	USC55 tests with Pre-production boards	85 days	Mon 15/08/05	Fri 09/12/05	62FS+10 days
64	FED Installation at USC55	180 days	Thu 17/11/05	Wed 26/07/06	58FF+30 days,62F
65	Tracker Installation	40 days	Mon 03/07/06	Fri 25/08/06	
66	First Power on Tracker	0 days	Tue 01/08/06	Tue 01/08/06	
67	LHC first run	30 days	Mon 02/04/07	Fri 11/05/07	
68					
69	Pb Free Directive in force	0 days	Sat 01/07/06	Sat 01/07/06	

FED Production Plans

Production Plans

Q3/2004 : Manufacture couple of FEDv2s. Done.

Q4/2004 : Testing FEDv2. Well advanced.

Manufacture of ~20 pre-production FEDv2s awaiting...

- S-LINK tests completion end Nov.
- QDR memories expected end Nov.
- Choice of optimal values for FE components end Nov?
- Tender quotes evaluation mid Nov.

- Launch pre-production mid Dec
- Assembled boards back starting Feb
- Commission boards and then full crate tests est. 10 weeks. If ok could start deliveries to CERN in May.

EU Tender Procedure for PCB/Assembly

Q3/2004 : Tender quotes (closing date 27 Oct).

Q4/2004 : Select company Nov. Further negotiations re Testing, delivery profiles. Arrange contract between CERN (on behalf of CMS FAs) and RAL.

Q1/2005 : Award contract with company Feb.

Q3/2005 -> Q3/2006 : Manufacture 500 FEDs; 20 off then @ ~ 50 / month. Fully test boards in UK. Ship to Prevessin B904; re-test full crates and store until USC55 available.

FED Availability Key Dates

Batches:

I) FEDv1 : 6 delivered already.*

II) FEDv2 : N Boards from pre-production run of ~20 ** available starting delivery in May 05

III) FEDv3 : N Boards from production validation run of ~20 available at (Tlaunch + 12 weeks) = end Oct 05

(both FEDv1 and FEDv2 can be used for LSA).

Every effort will be made to meet realistic delivery schedules for LSA once known to us.
Some very limited flexibility to advance dates.

Options?

* 2 more FEDv1 possible with a little effort if urgently needed.

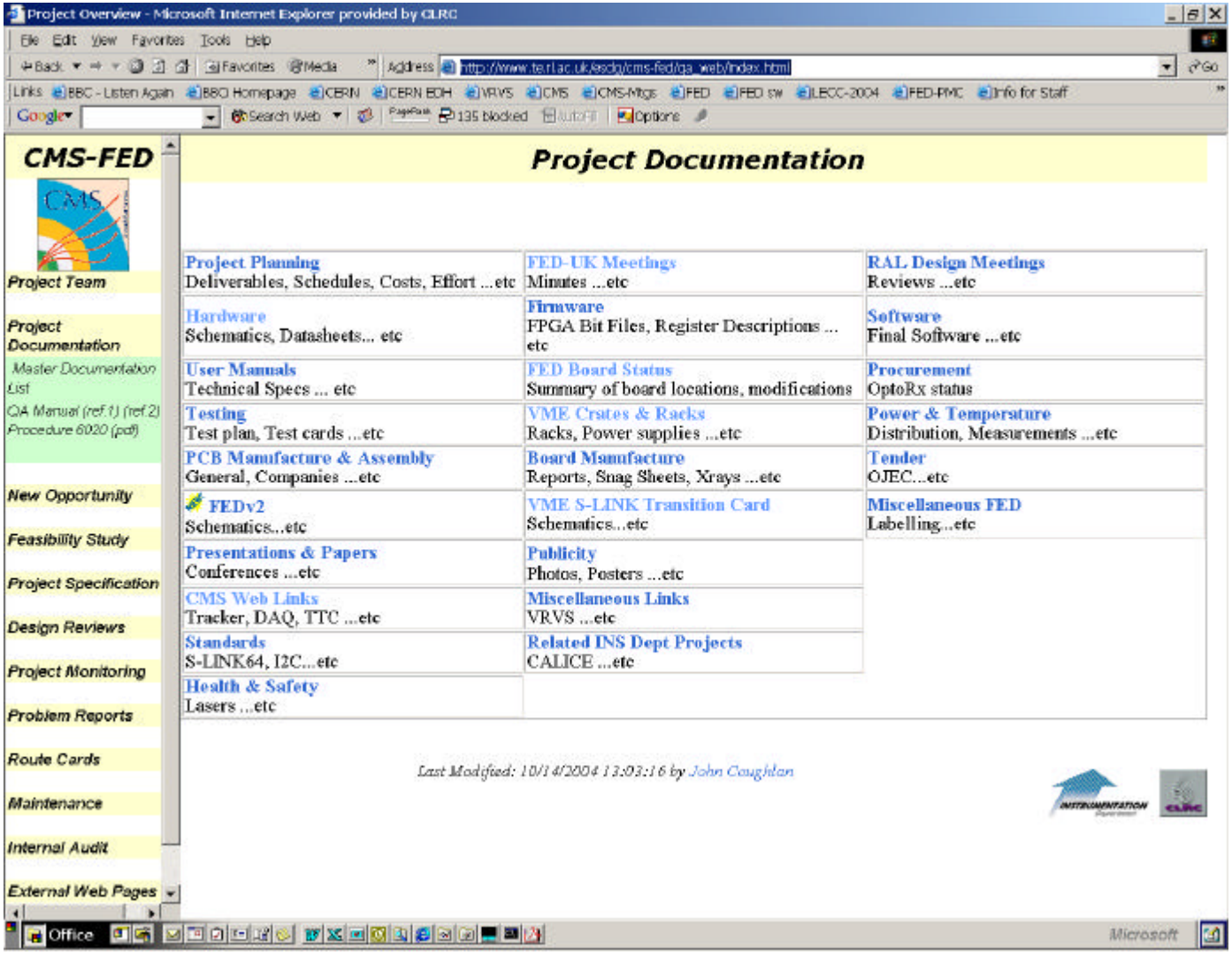
** Make ~ 25 pre-production FEDv2 if sufficient kit is in hand.

Risk if insufficient time is allowed for full crate tests.

Assuming full crate tests verify FEDv2 design.

LSA boards to be recycled to USC55 ? Treated as spares ?

FED web pages



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