

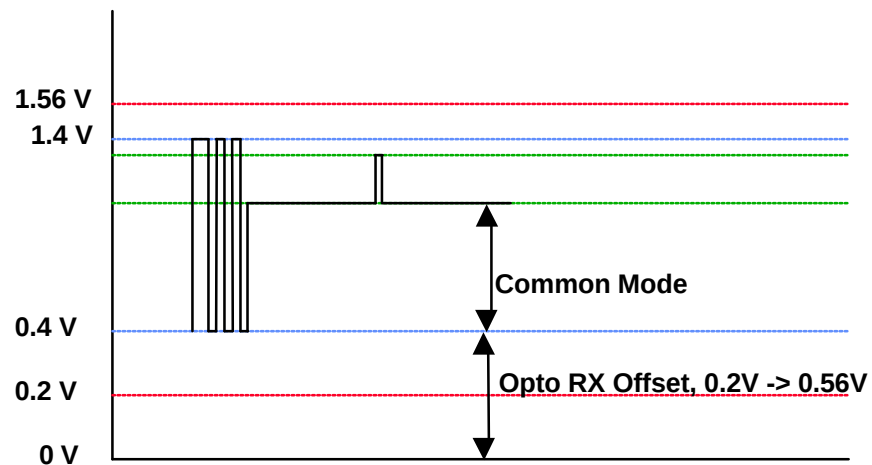
CMS Tracker FED Front End Module Analogue Circuit Options

Draft 1.0

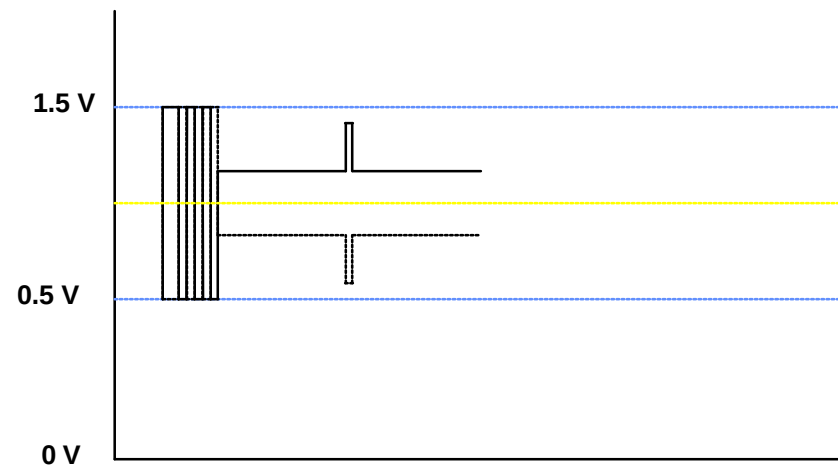


Signal Ranges

Opto RX Output



ADC Input



- Limits of Opto Rx Output, assuming default opto settings - see below
- 1V range of header/signal + common mode -> 10 bit, 1 mV/bit
- 0.25V range of signal -> 8 bit, 1mV/bit

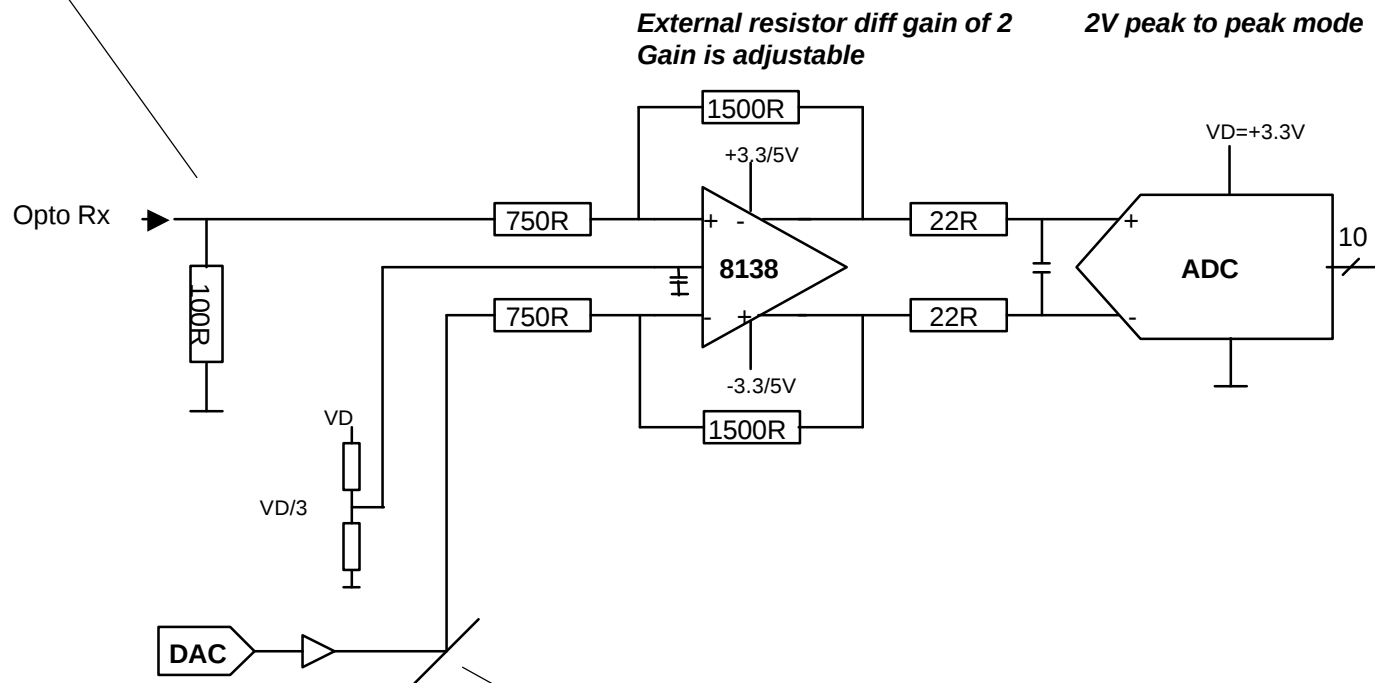
Assume Opto Rx Offset voltage closely matched across all 12 channels

Default Opto Rx Controls = 000110



Single Stage AD8138 or equivalent

High AC current fed back to Opto Rx Output
DC Currents effecting operating point
Opto Rx output is a current source not voltage source

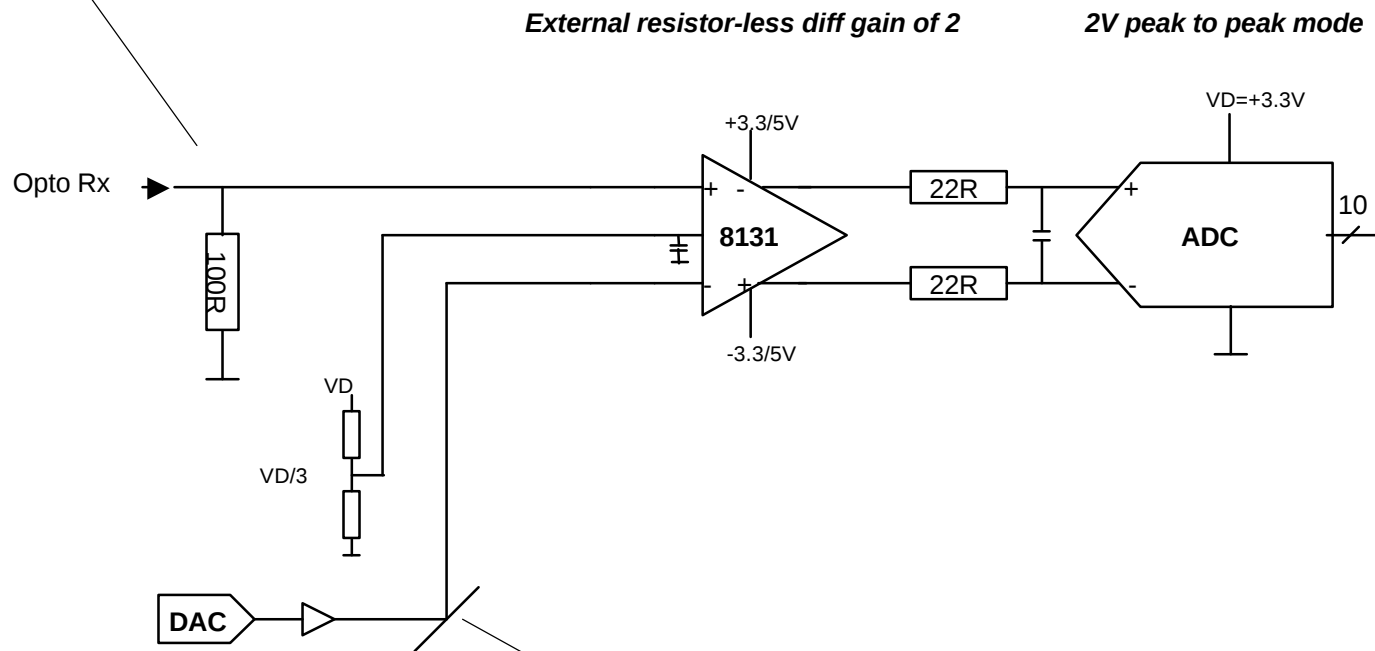


High AC currents fed back through feedback resistors
Causes Ripple Problem - couples directly to output
Point needs less than half LSB ripple ~500 μ V
Common to up to 12 channels in module
Possible cross talk between channels



Single Stage AD8131 or equivalent

High AC current fed back to Opto Rx Output
DC Currents effecting operating point
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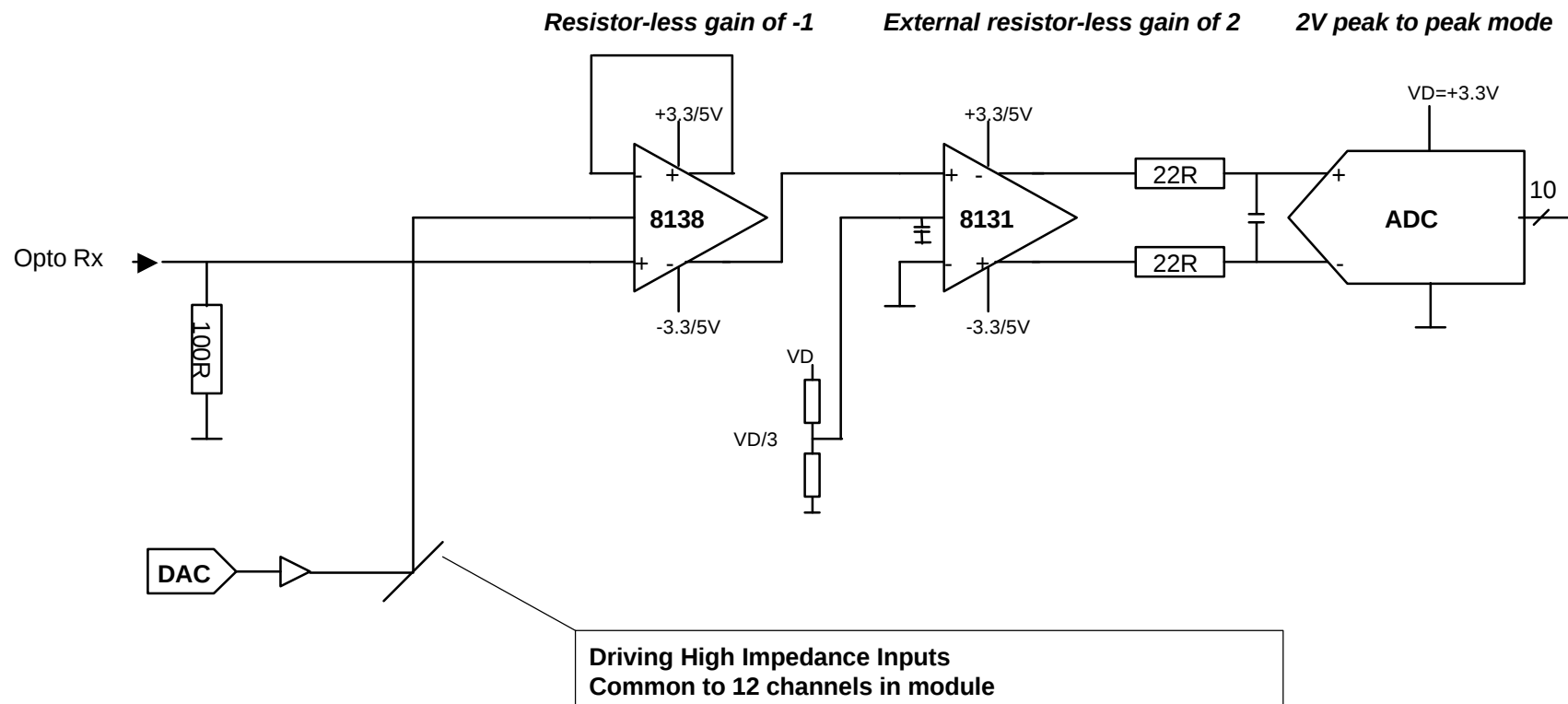


Ripple Problem - couples directly to output
Point needs less than half LSB ripple $\sim 500\mu\text{V}$
High AC currents fed back through feedback resistors
Common to up to 12 channels in module
Possible cross talk between channels

Two Stage AD8138-8131 or equivalents

$$\begin{aligned} V_{out+} &= V_{in+} \\ V_{out-} &= 2 V_{OCM} - V_{in+} \end{aligned}$$

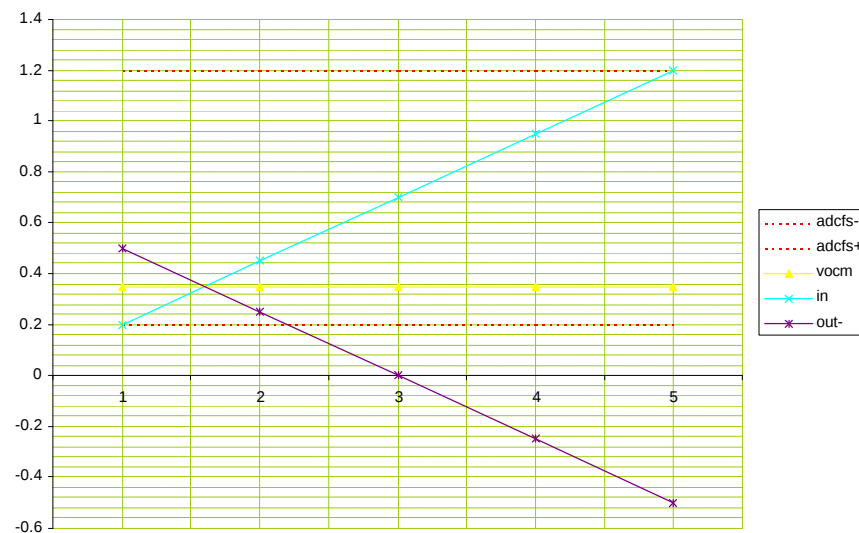
$$\begin{aligned} V_{out+} &= V_{OCM} + V_{in+} \\ V_{out-} &= V_{OCM} - V_{in+} \end{aligned}$$





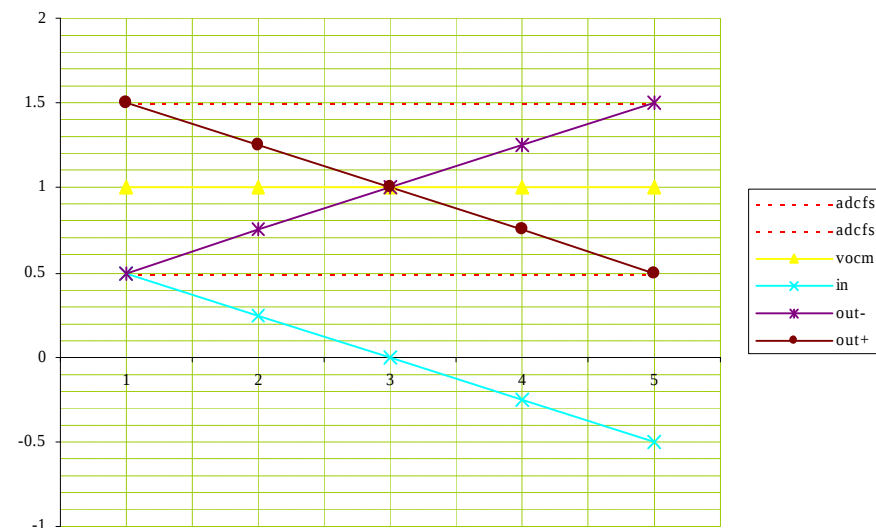
Two stage transfer functions example

AD8138



Opto Rx Output Offset of 0.2V
Signal swing of 1V

AD8131

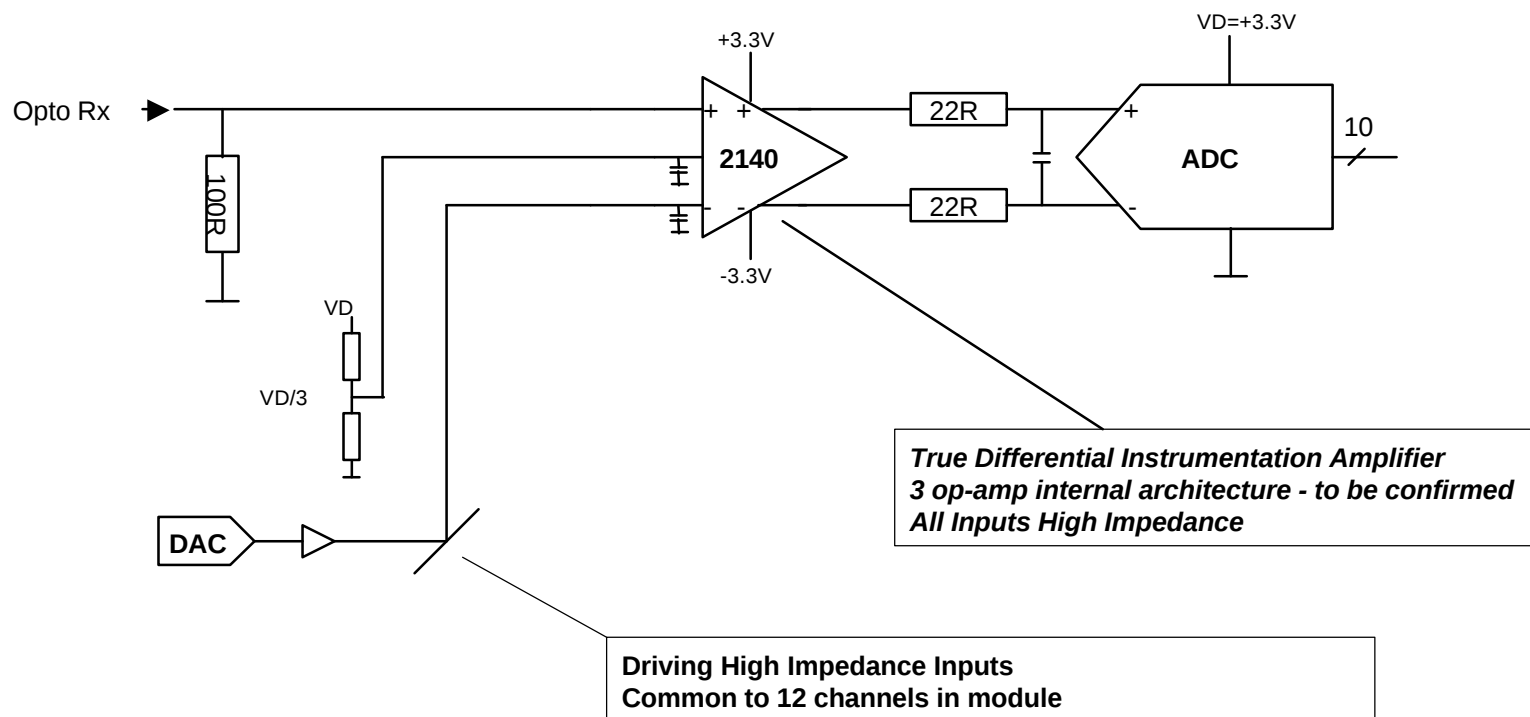


ADC in 2 VPP Mode
ADC Common Mode $V_{DD}/3 = 1V$



Single Stage EL2140 or equivalent

External resistor- less gain of 2 2V peak to peak mode





Summary

	<u>AD8131/8</u>	<u>AD8131 & 8</u>	<u>EL2140C</u>
Approach	1 stage	2 Stage	1 Stage
Amp type	Diff	Diff	Diff Instr
Amp Gain Adj	Yes/No	No	No
Ripple	>= LSB	<<LSB	<<LSB
Power Estimate*	85W	95W	75W
Cost	Low/Mod	High	Low
Vendor	Major	Major	Intersil
Second Source	TI	TI	No?
Package	μSOIC	μSOIC	SOIC
Sim Model	Yes	Yes	Yes

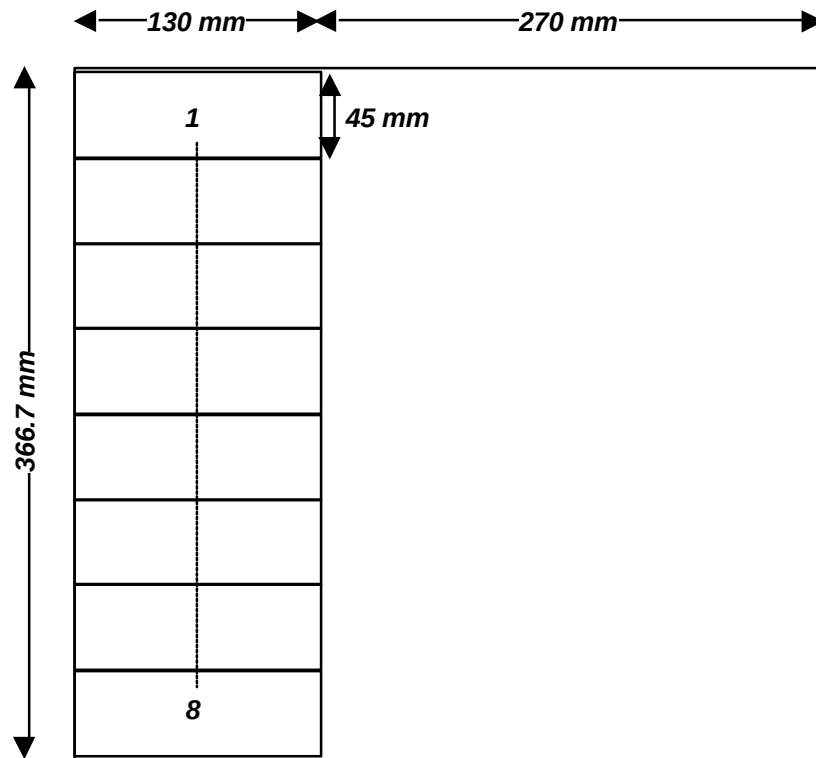
EL2140C - needs further study?

*** Estimated FED Power - still under study**



9U Board Layout

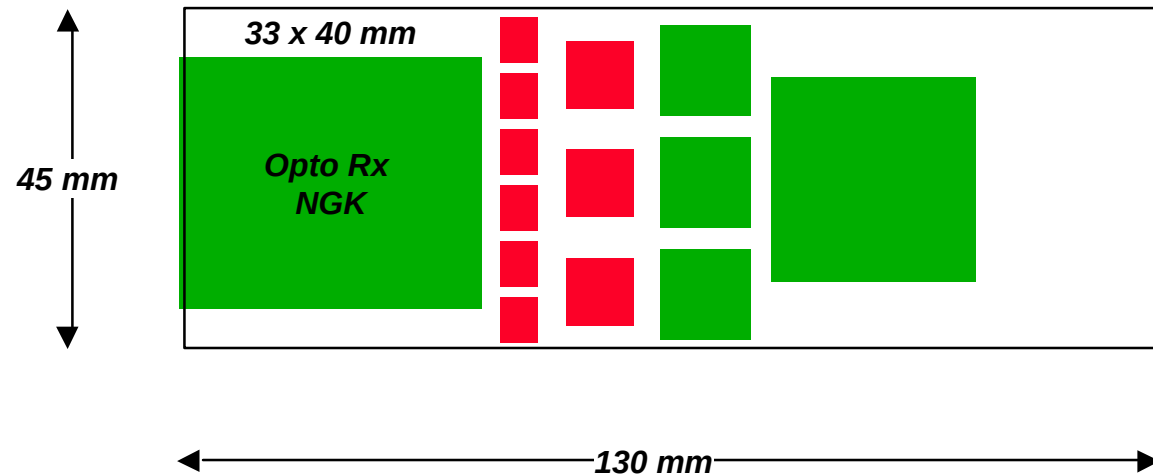
Front End Envelope



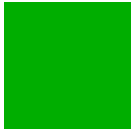


Front End Module Layout

EL2140/XC2V40/XC2V2000



N.B. No Passives Shown

27 x 27 mm		FPGA XC2V1000- XC2V3000 FG676
12 x 12mm		FPGA XC2V40 CS144
9 x 9 mm		ADC AD9218 ST48
5 x 3 mm		DIFF OP-AMP AD9218 RM8 - μ SOIC
5 x 6 mm		DIFF OP-AMP EL2140 SOIC
17 x 17mm		FPGA XC2V250 FG256

Double Sided

Single Sided