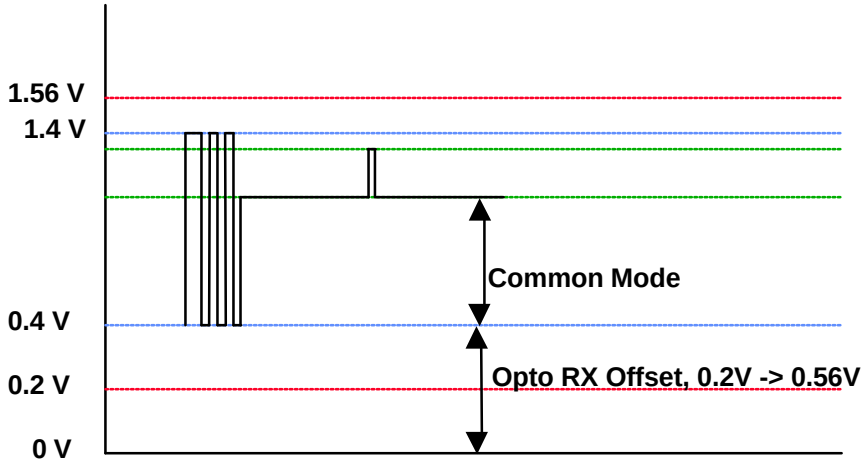
CMS Tracker FED Front End Module Analogue Circuit Considerations

Draft 1.0

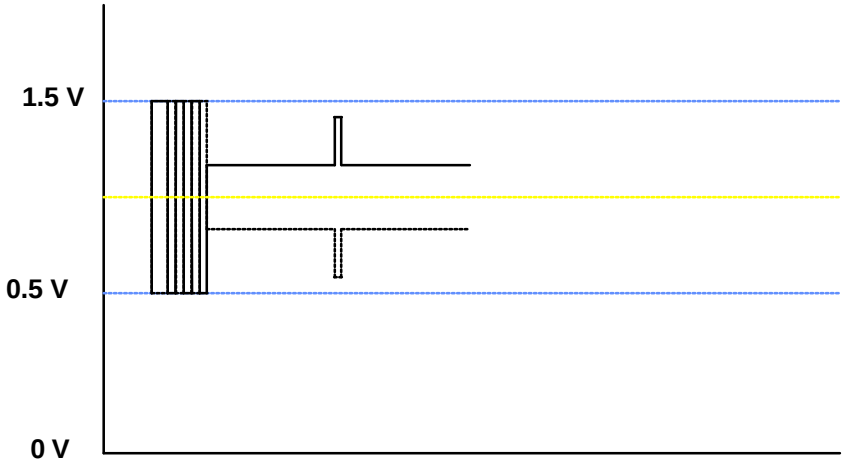
Rob Halsall et al.

Signal Ranges

Opto RX Output



ADC Input



Limits of Opto Rx Output, assuming default opto settings - see below

1V range of header/signal + common mode -> 10 bit, 1 mV/bit

0.25V range of signal -> 8 bit, 1mV/bit

Assume Opto Rx Offset voltage closely matched across all 12 channels

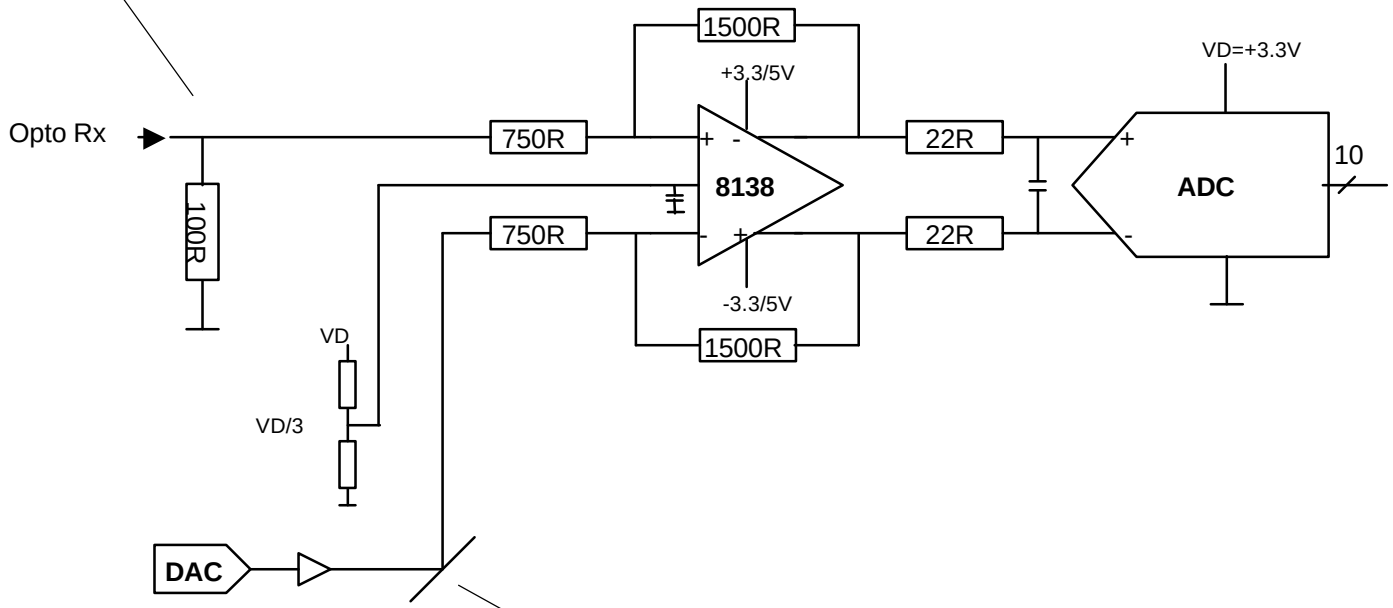
Default Opto Rx Controls = 000110

Single Stage AD8138 or equivalent

High AC current fed back to Opto Rx Output
DC Currents effecting operating point
Opto Rx ouput is a current source not voltage source

External resistor diff gain of 2
Gain is adjustable

2V peak to peak mode

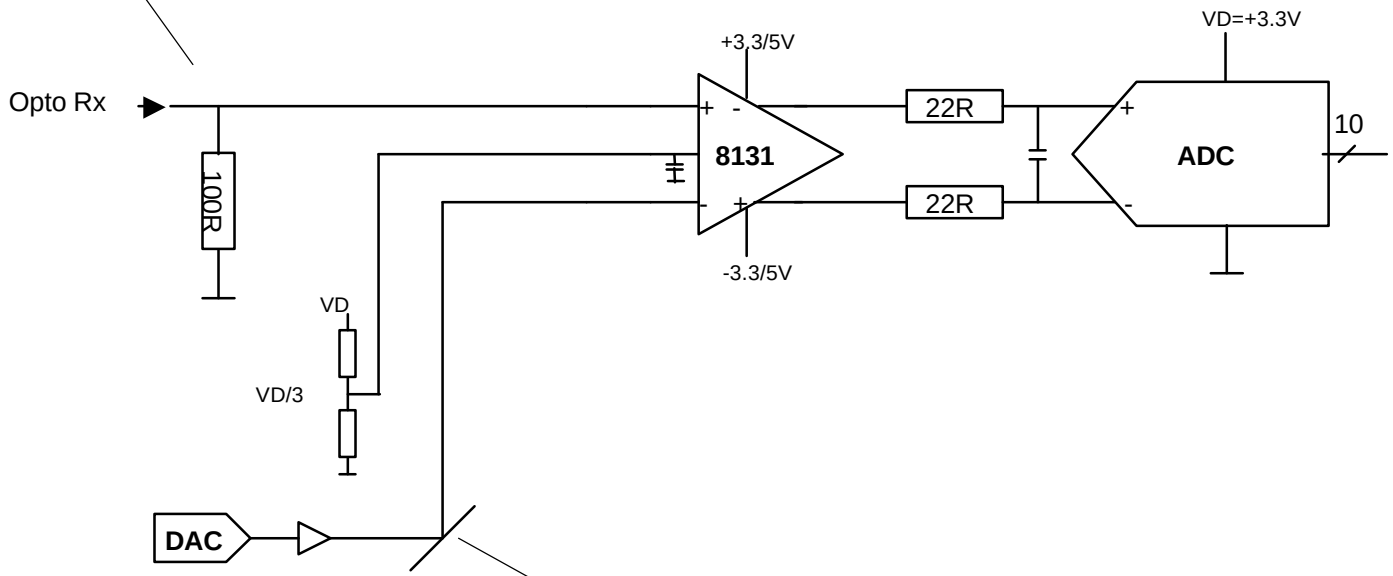


High AC currents fed back through feedback resistors
Causes Ripple Problem - couples directly to output
Point needs less than half LSB ripple ~500µV
Common to up to 12 channels in module
Possible cross talk between channels

Single Stage AD8131 or equivalent

High AC current fed back to Opto Rx Output
DC Currents effecting operating point
Opto Rx ouput is a current source not voltage source

External resistor-less diff gain of 2 ***2V peak to peak mode***



Ripple Problem - couples directly to output
Point needs less than half LSB ripple ~500µV
High AC currents fed back through feedback resistors
Common to up to 12 channels in module
Possible cross talk between channels

Two Stage AD8138-8131 or equivalents

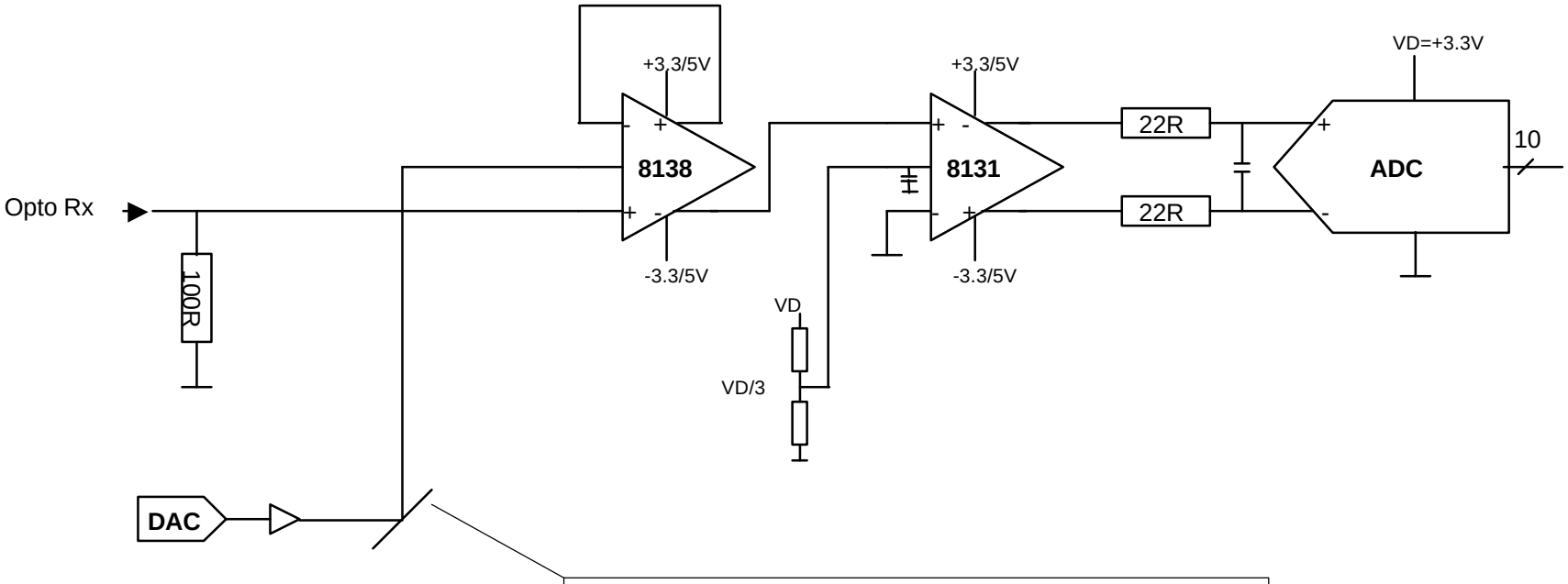
Vout+ = Vin+
Vout- = 2 VOCM - Vin+

Vout+ = VOCM + Vin+
Vout- = VOCM - Vin+

Resistor-less gain of -1

External resistor-less gain of 2

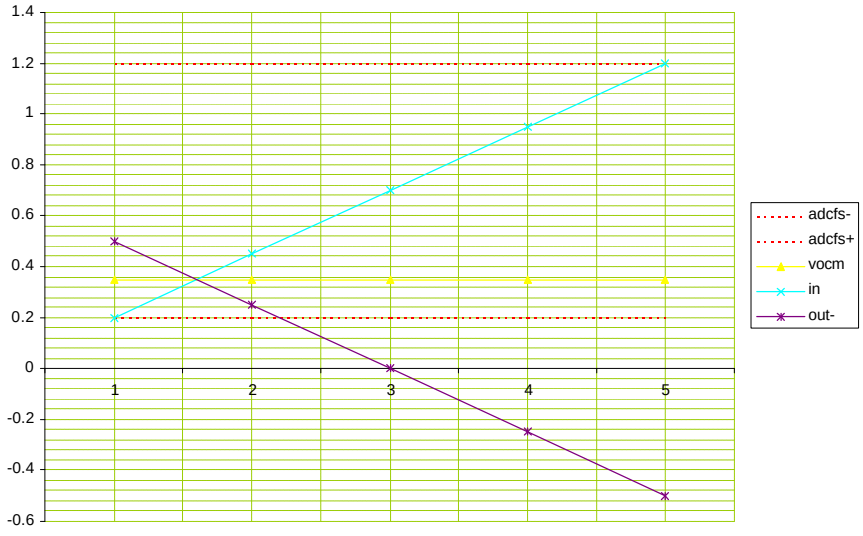
2V peak to peak mode



Driving High Impedance Inputs
Common to 12 channels in module

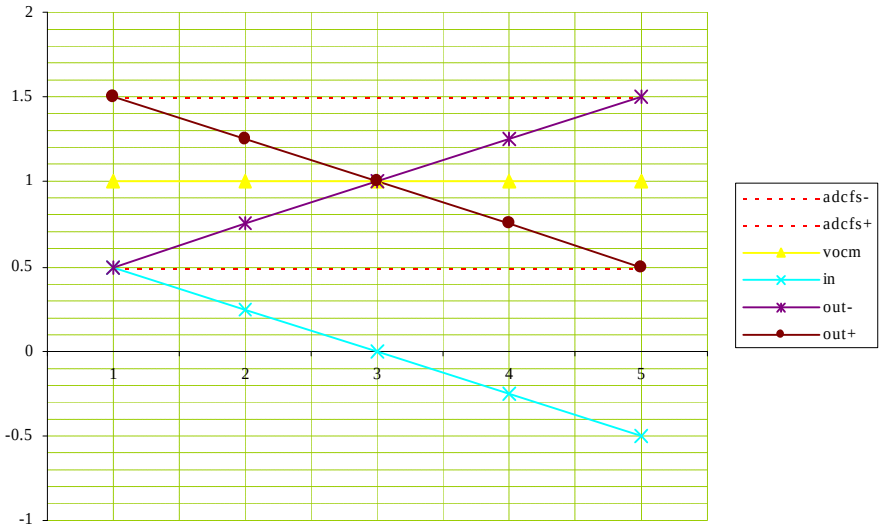
Two stage transfer functions example

AD8138



Opto Rx Output Offset of 0.2V
Signal swing of 1V

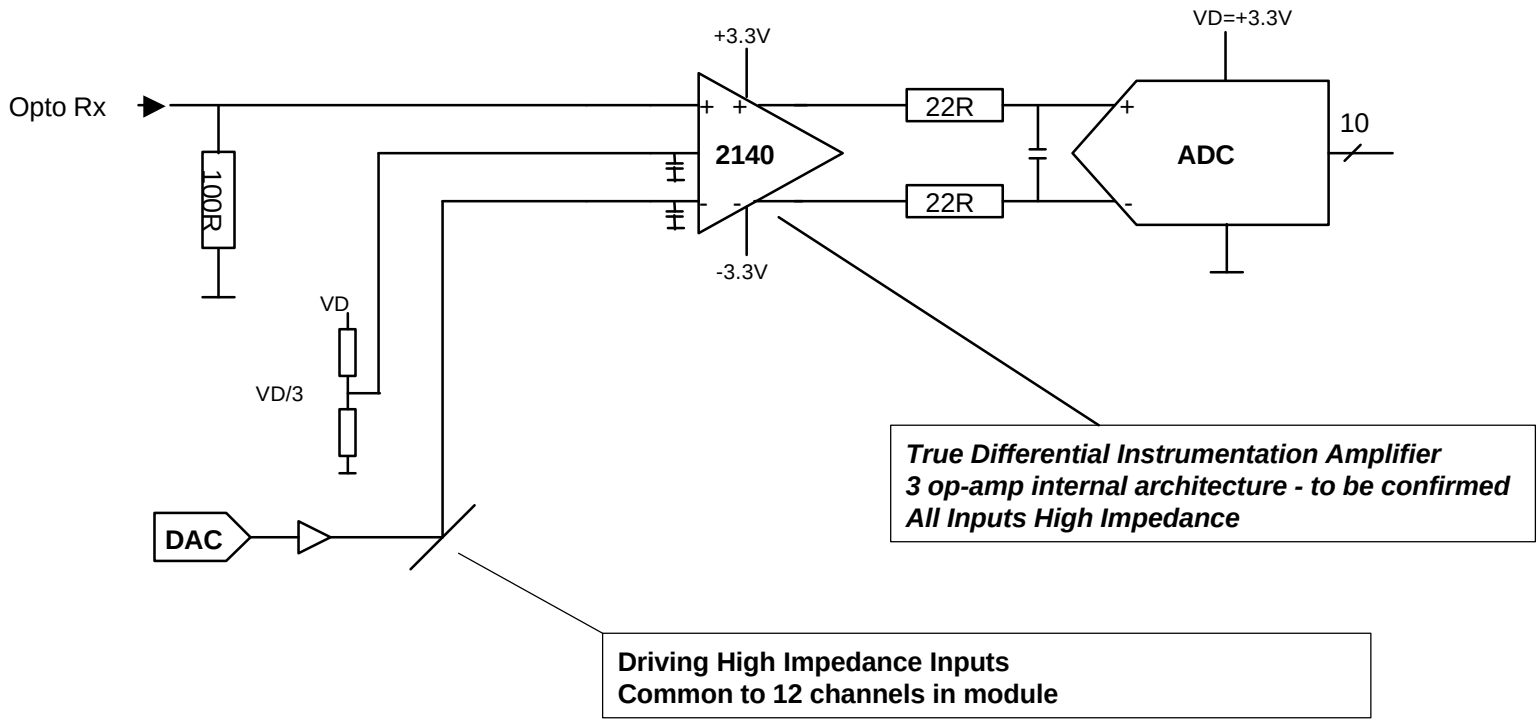
AD8131



ADC in 2 VPP Mode
ADC Common Mode VDD/3 = 1V

Single Stage EL2140 or equivalent

External resistor- less gain of 2 ***2V peak to peak mode***



Summary

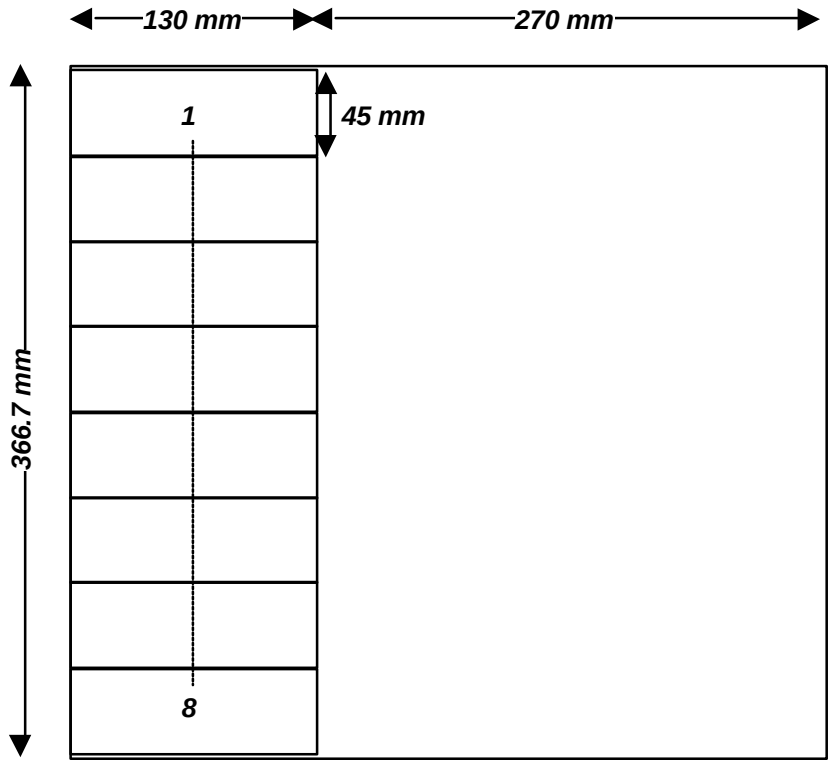
	AD8131/8	AD8131 & 8	EL2140C
Approach	1 stage	2 Stage	1 Stage
Amp type	Diff	Diff	Diff Instr
Amp Gain Adj	Yes/No	No	No
Ripple	>= LSB	<<LSB	<<LSB
Power Estimate*	85W	95W	75W
Cost	Low/Mod	High	Low
Vendor	Major	Major	Intersil
Second Source	TI	TI	No?
Package	µSOIC	µSOIC	SOIC
Sim Model	Yes	Yes	Yes

EL2140C - needs further study?

* Estimated FED Power - still under study

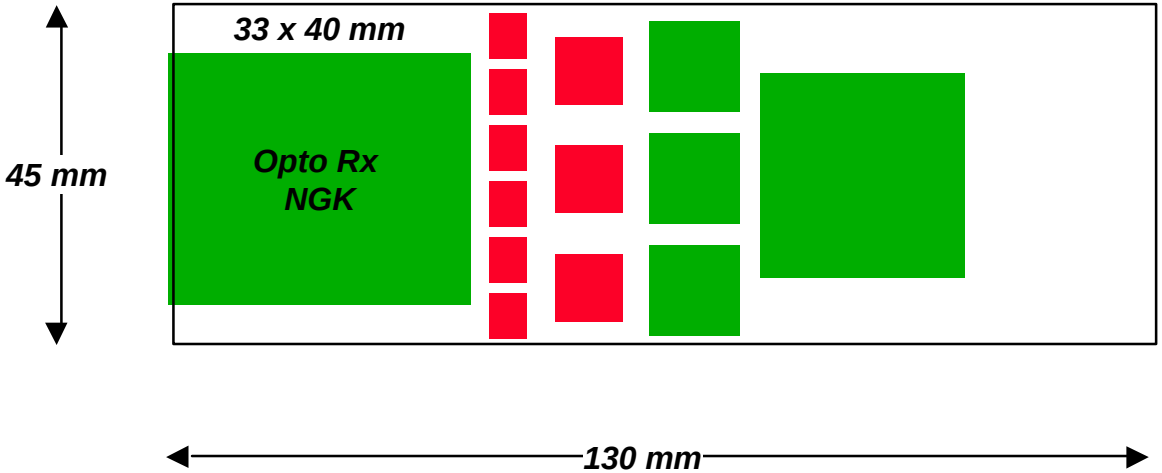
9U Board Layout

Front End Envelope

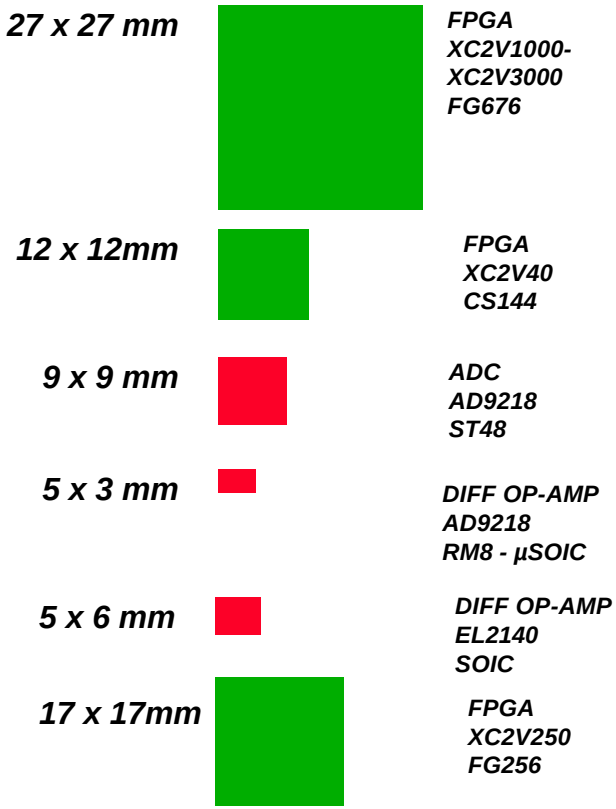


Front End Module Layout

EL2140/XC2V40/XC2V2000



N.B. No Passives Shown



Double Sided

Single Sided