CMS-FED PC3205M Test Specification for DDi Technologies

Document History

V1.0	22.06.04	JAC	Skeleton draft.
V2.0	10.11.04	ITC	Added test procedures up to and including Boundary Scan.
V2.1	11.11.04	JAC	added comments.

Introduction

The CMS-FED is a 9U x 400 mm VME64x board (Figures 1 & 2) used to readout data from the CMS experiment at CERN Geneva. A total of 500 boards are required for the complete readout system.

This document describes the testing station and commissioning procedures to be performed at DDi Technologies in order to verify the manufacture of CMS FED PC3205M prior to delivery to RAL. These tests are to be performed after the standard Quality Assurance methods such as Automated Optical Inspection and X-Ray/Ersascope inspection described elsewhere [1].

It is assumed that the procedures described will be carried out by technicians employed at DDi following basic training by RAL staff and that thereafter only minimal supervision and support should be necessary.

The connectivity of the digital components will be verified by means of standard JTAG Boundary Scan. The connectivity of the analogue circuitry and the verification of the board operation will be carried out by standalone VME crate based tests using a test station provided to DDi. The latter tests will be carried out using VME readout but without the use of optical input signals.

The results of the Boundary Scan, and Analogue tests and the visual checks of the operators will be recorded in the FED Route Card Online Database along with details of any repair work carried out.

The final system tests, using optical inputs and fully populated crates, will subsequently be carried out at RAL. Boards will then be shipped to CERN for final CMS readout integration tests at Prevessin B904 before installation at USC55. These tests and the associated evaluation of the hardware and firmware design are beyond the scope of the present document.

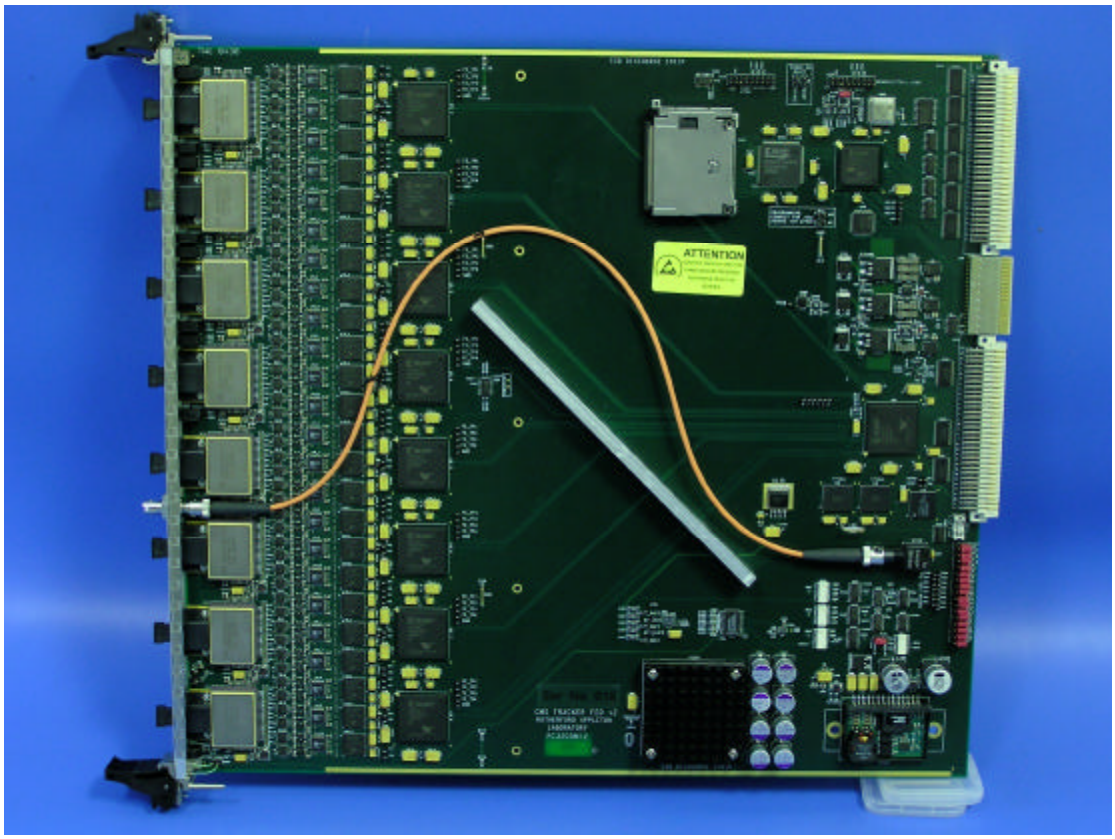


Figure 1 : CMS-FED PC3205M/2 primary side (N.B. optical fibre and front panel connector shown will not be present at DDi)

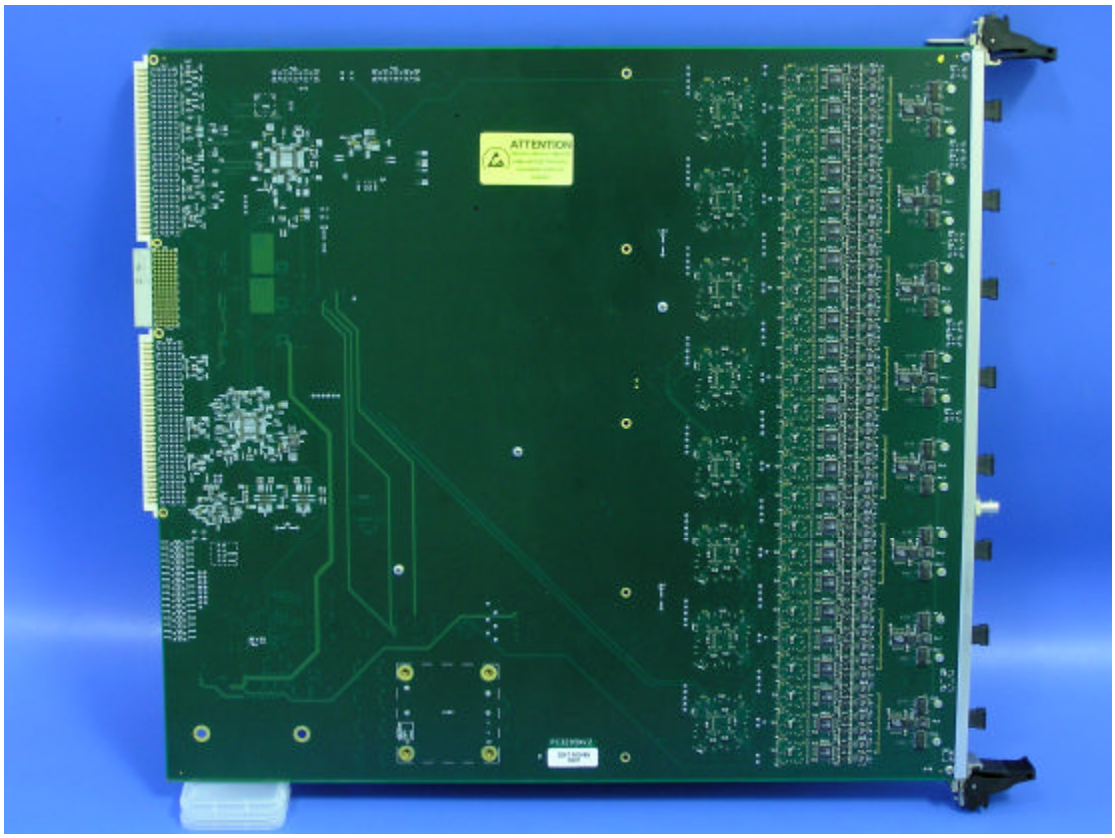


Figure 2 : CMS-FED PC3205M/2 secondary side

Test Set-ups

The proposed set-ups are shown below:

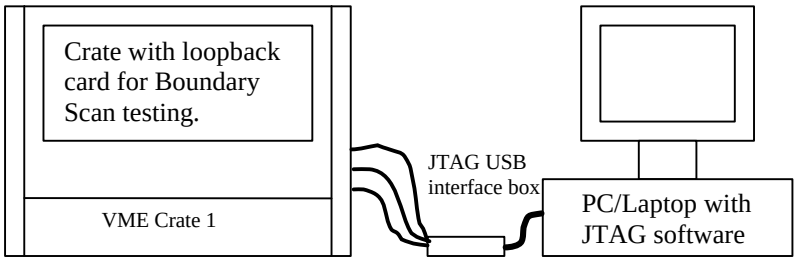


Figure 3 : Boundary Scan test set-up

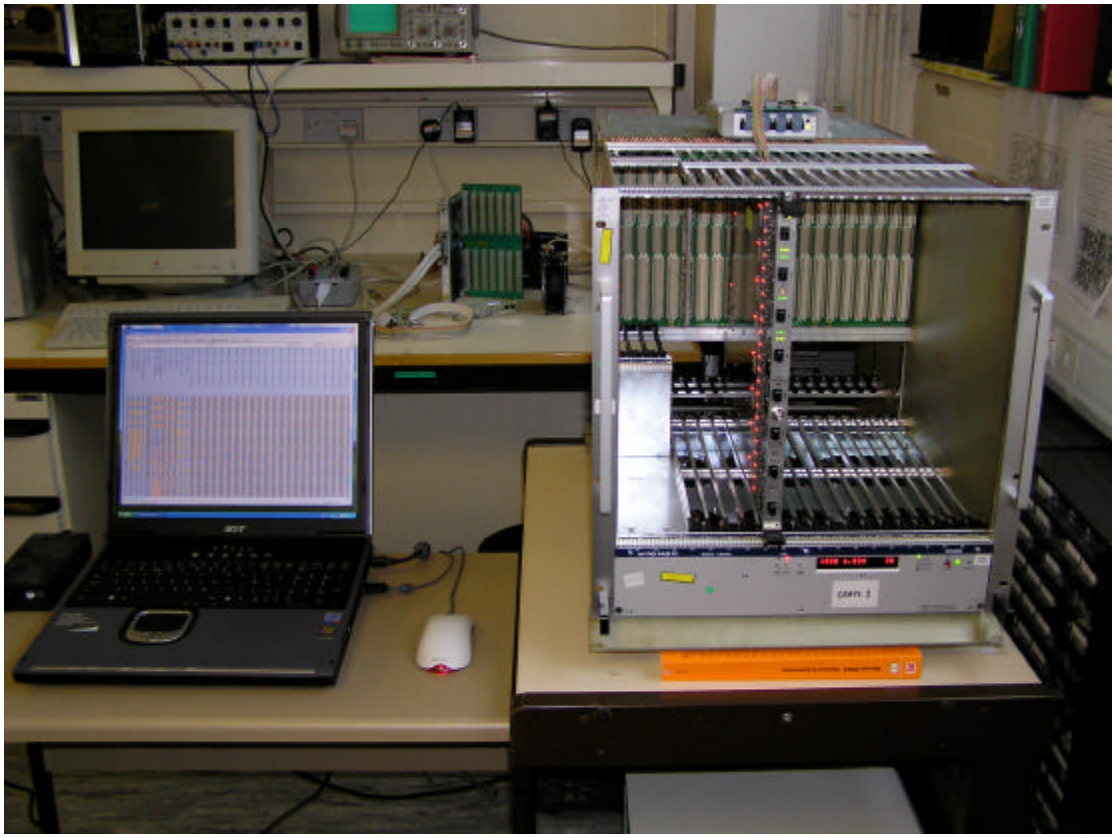


Figure 4 : Image of existing RAL Boundary Scan set-up

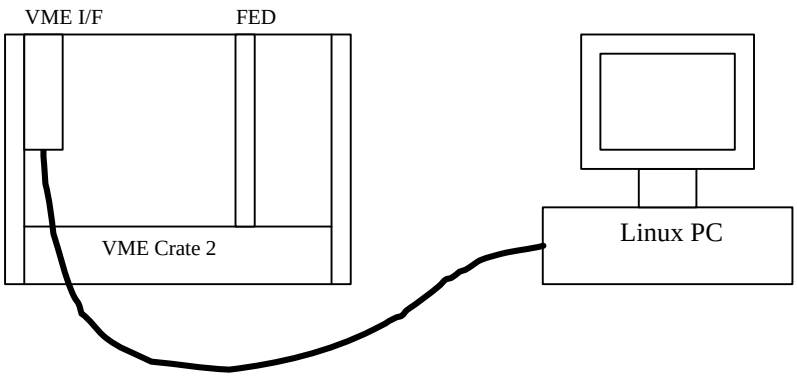


Figure 5 : VME readout test set-up

The equipment to be provided by RAL to DDi are listed below:

Item	Comment
LHC standard 9U crates.	Two off, one for the Boundary Scan and one for VME testing.
PC running Linux.	CERN Red Hat Linux
PC-VME interface cards.	SBS or CAEN
Loop back card and cables for Boundary Scan	Loop back card is used to test as many as possible of the J1 and J2 connections on the FED and is plugged into an adjacent slot on the front of the backplane.
PC/laptop with Boundary Scan system installed on it, and USB splitter box to generate the four boundary scan chains.	JTAG Systems to match RAL system. May be available at DDi?
Boundary Scan files.	
Bar codes & 2D barcode reader.	E.g.
Compact flash cards & Files	

N.B. Identical set-ups will also be required at RAL and CERN.

Test Procedures

The results at each step of test procedures described in the following sections (Figure 6) are entered into the LabView program (section N) for storage in the online Route Card Database.

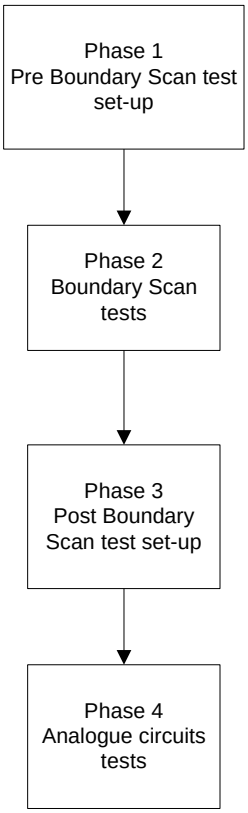
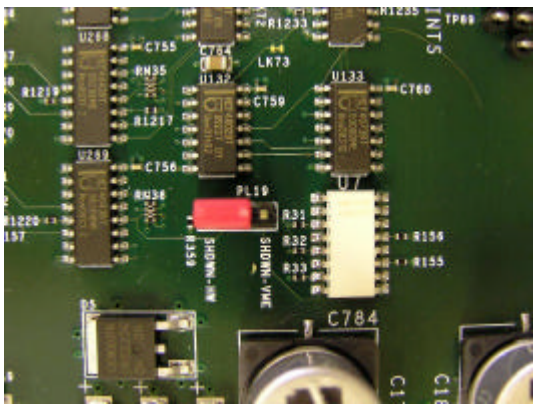


Figure 6 : Test procedures Phases

Phase 1: Pre Boundary Scan test set-up

1. Fit serial number to PCB
2. Visual inspection
3. Fit 1.5A fuse
4. Check for short circuits on the supplies with a multimeter.
5. Fit front panel.
6. Fit shorting links for testing (image 1.1, 1.2 & 1.3).
7. Insert carefully into Boundary Scan test crate and check that the card inserts and extracts correctly.
8. Power on the crate and verify that the card powers successfully by checking the LED status (image 1 .4), all LEDs off.



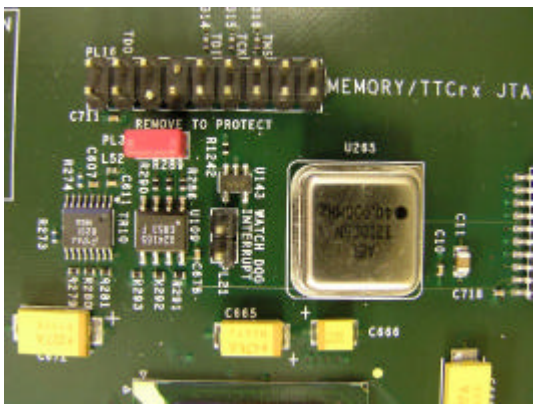


image 1.1

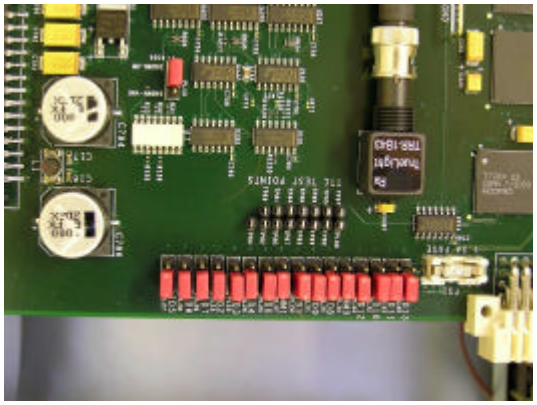


image 1.2

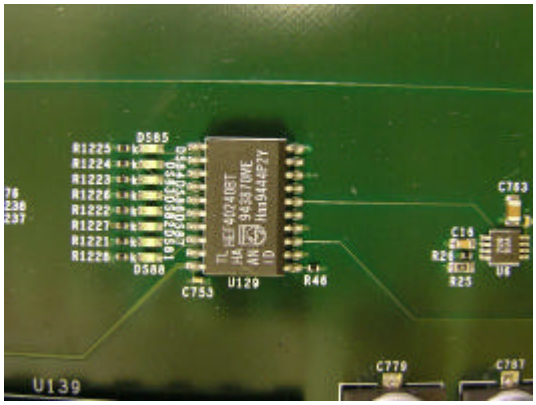


image 1.3

image 1.4

Phase2: Boundary Scan tests

1. Run Vip 3.2 software.
2. Select ident test and run. This will check the identity of the devices in the JTAG chains. Note 1
3. Select inter test and run. This will check the interconnection of the devices in the JTAG chains. Note 1

Note 1. More details of the interpretation of the software results are discussed later.

Phase3: Post Boundary Scan test set-up

1. Fit front panel serial number label.
2. Attach 2D barcode to front panel and record details (image 1.5).
3. Wire front panel extract switch (image 1.6).
4. Fit diagonal air deflector bar (image 1.7).
5. Plug-in programmed compact flash card.
6. Insert into system test crate and power on.
7. Connect Xilinx “parallel 3” cable to the VME Boundary Scan connector and program the VME PROM device.
8. Re-boot PC3205 card by pressing the restart button and check to see that DS1_X, DS2_X, DS5_X, and DS7_X are all flashing.

image 1.5

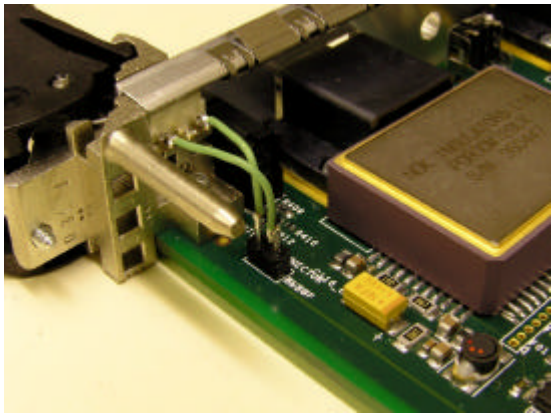


image 1.6

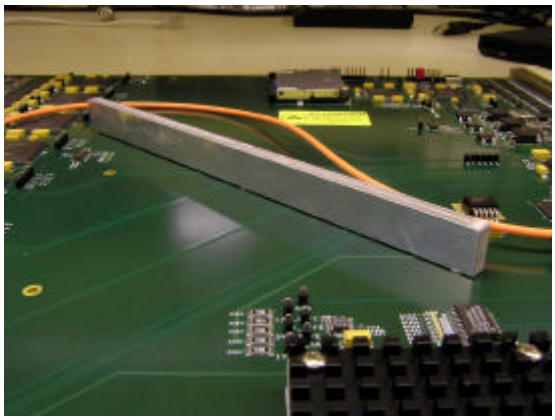


image 1.7

Phase 4: Analogue circuits test

Test Software

The test software is a LabView based program running under Linux.

The operator interface GUI is illustrated in Figure N.

References

[1] DDi Production Report for PC3205M/1, March 2004