CHANNEL 1 — I10

FED_CHANNEL

BCLK_LVDS<1>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD1_DATA_STREAM<0..3>
ICLK_LVDS<1>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<1>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<1>
FRAME_SYNC_IN<1>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<1>
CONFIG_IN<1>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<1>
MONITOR_IN<1>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<1>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_1#
CF1_TDI	FE_TDI	FE_TDO	CF1_TD1
CF1_TMS	FE_TMS		
CF1_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE1_DONE

CHANNEL 2 — I11

FED_CHANNEL

BCLK_LVDS<2>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD2_DATA_STREAM<0..3>
ICLK_LVDS<2>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<2>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<2>
FRAME_SYNC_IN<2>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<2>
CONFIG_IN<2>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<2>
MONITOR_IN<2>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<2>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_2#
CF1_TDI	FE_TDI	FE_TDO	CF1_TD2
CF1_TMS	FE_TMS		
CF1_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE2_DONE

CHANNEL 3 — I12

FED_CHANNEL

BCLK_LVDS<3>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD3_DATA_STREAM<0..3>
ICLK_LVDS<3>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<3>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<3>
FRAME_SYNC_IN<3>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<3>
CONFIG_IN<3>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<3>
MONITOR_IN<3>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<3>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_3#
CF1_TD2	FE_TDI	FE_TDO	CF1_TD3
CF1_TMS	FE_TMS		
CF1_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE3_DONE

CHANNEL 4 — I13

FED_CHANNEL

BCLK_LVDS<4>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD4_DATA_STREAM<0..3>
ICLK_LVDS<4>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<4>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<4>
FRAME_SYNC_IN<4>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<4>
CONFIG_IN<4>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<4>
MONITOR_IN<4>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<4>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_4#
CF1_TD3	FE_TDI	FE_TDO	CF1_TD4
CF1_TMS	FE_TMS		
CF1_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE4_DONE

CHANNEL 5 — I14

FED_CHANNEL

BCLK_LVDS<5>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD5_DATA_STREAM<0..3>
ICLK_LVDS<5>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<5>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<5>
FRAME_SYNC_IN<5>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<5>
CONFIG_IN<5>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<5>
MONITOR_IN<5>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<5>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_5#
CF2_TDI	FE_TDI	FE_TDO	CF2_TD1
CF2_TMS	FE_TMS		
CF2_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE5_DONE

CHANNEL 6 — I15

FED_CHANNEL

BCLK_LVDS<6>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD6_DATA_STREAM<0..3>
ICLK_LVDS<6>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<6>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<6>
FRAME_SYNC_IN<6>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<6>
CONFIG_IN<6>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<6>
MONITOR_IN<6>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<6>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_6#
CF2_TD1	FE_TDI	FE_TDO	CF2_TD2
CF2_TMS	FE_TMS		
CF2_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE6_DONE

CHANNEL 7 — I16

FED_CHANNEL

BCLK_LVDS<7>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD7_DATA_STREAM<0..3>
ICLK_LVDS<7>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<7>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<7>
FRAME_SYNC_IN<7>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<7>
CONFIG_IN<7>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<7>
MONITOR_IN<7>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<7>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_7#
CF2_TD2	FE_TDI	FE_TDO	CF2_TD3
CF2_TMS	FE_TMS		
CF2_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE7_DONE

CHANNEL 8 — I17

FED_CHANNEL

BCLK_LVDS<8>	B_CLOCK_LVDS_IN	DATA_STREAM<0..3>	MOD8_DATA_STREAM<0..3>
ICLK_LVDS<8>	I_CLOCK_LVDS_IN		
READOUT_SYNC_IN<8>	READOUT_SYNC_IN	READOUT_SYNC_OUT	READOUT_SYNC_OUT<8>
FRAME_SYNC_IN<8>	FRAME_SYNC_IN	FRAME_SYNC_OUT	FRAME_SYNC_OUT<8>
CONFIG_IN<8>	CONFIG_IN	CONFIG_OUT	CONFIG_OUT<8>
MONITOR_IN<8>	MONITOR_IN	MONITOR_OUT	MONITOR_OUT<8>
+5V	+5VA	FULL_FLAG	FULL_FLAG
5VA_NEG	5VA_NEG	HALF_FLAG	HALF_FLAG
1V5	1V5	EMPTY_FLAG	EMPTY_FLAG
3V3	3V3	FE_INT#	TEMP_INT#
GND	GND	FE_T_CRIT#	T_CRIT_8#
CF2_TD3	FE_TDI	FE_TDO	CF2_TD4
CF2_TMS	FE_TMS		
CF2_TCK	FE_TCK	CFG_PROG_B	CFG_PROG_B
		CFG_INIT#	CFG_INIT#
		FE_DONE	FE8_DONE

I9

FED_BACKEND

MOD1_DATA_STREAM<0..3>	MOD1_DATA_STREAM<0..3>		
MOD2_DATA_STREAM<0..3>	MOD2_DATA_STREAM<0..3>	BCLK_LVDS_OUT<1..8>	BCLK_LVDS<1..8>
MOD3_DATA_STREAM<0..3>	MOD3_DATA_STREAM<0..3>	ICLK_LVDS_OUT<1..8>	ICLK_LVDS<1..8>
MOD4_DATA_STREAM<0..3>	MOD4_DATA_STREAM<0..3>		
MOD5_DATA_STREAM<0..3>	MOD5_DATA_STREAM<0..3>		
MOD6_DATA_STREAM<0..3>	MOD6_DATA_STREAM<0..3>		
MOD7_DATA_STREAM<0..3>	MOD7_DATA_STREAM<0..3>		
MOD8_DATA_STREAM<0..3>	MOD8_DATA_STREAM<0..3>		
READOUT_SYNC_OUT<1..8>	READOUT_SYNC_OUT<1..8>	READOUT_SYNC_IN<1..8>	READOUT_SYNC_IN<1..8>
FRAME_SYNC_OUT<1..8>	FRAME_SYNC_OUT<1..8>	FRAME_SYNC_IN<1..8>	FRAME_SYNC_IN<1..8>
CONFIG_OUT<1..8>	CONFIG_OUT<1..8>	CONFIG_IN<1..8>	CONFIG_IN<1..8>
MONITOR_OUT<1..8>	MONITOR_OUT<1..8>	MONITOR_IN<1..8>	MONITOR_IN<1..8>
FULL_FLAG	FULL_FLAG		
HALF_FLAG	HALF_FLAG		
EMPTY_FLAG	EMPTY_FLAG		
TEMP_INT#	TEMP_INT#		
T_CRIT_1#	T_CRIT_1#	+5V	+5V
T_CRIT_2#	T_CRIT_2#	5VA_NEG	5VA_NEG
T_CRIT_3#	T_CRIT_3#	3V3	3V3
T_CRIT_4#	T_CRIT_4#	1V5	1V5
T_CRIT_5#	T_CRIT_5#	GND	GND
T_CRIT_6#	T_CRIT_6#		
T_CRIT_7#	T_CRIT_7#		
T_CRIT_8#	T_CRIT_8#		
FE1_DONE	FE1_DONE		
FE2_DONE	FE2_DONE		
FE3_DONE	FE3_DONE		
FE4_DONE	FE4_DONE		
FE5_DONE	FE5_DONE		
FE6_DONE	FE6_DONE		
FE7_DONE	FE7_DONE		
FE8_DONE	FE8_DONE		
CF1_TD4	CF1_TD4	CF1_TDI	CF1_TDI
		CF1_TMS	CF1_TMS
		CF1_TCK	CF1_TCK
CF2_TDO	CF2_TDO	CF2_TDI	CF2_TDI
		CF2_TMS	CF2_TMS
		CF2_TCK	CF2_TCK
CFG_PROG_B	CFG_PROG_B		
CFG_INIT#	CFG_INIT#		

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

© CCLRC 2002

CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED v1

TOP LEVEL

A | 2-TE-0070-020-01-A

TOTAL NO. OF SHEETS 95

A | 2-TE-0070-020-01-A