A	2-TE-0070-020-01-B	THIS DRAWING CONFORMS TO B.S. 3939	

CHANNEL 1

I10

FED_CHANNEL

BCLK_LVDS<1>
ICLK_LVDS<1>
READOUT_SYNC_IN<1>
FRAME_SYNC_IN<1>
CONFIG_IN<1>
MONITOR_IN<1>
+5V
5VA_NEG
1V5
3V3
GND
CF1_TDI
CF1_TMS
CF1_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD1_DATA_STREAM<0..3>
READOUT_SYNC_OUT<1>
FRAME_SYNC_OUT<1>
CONFIG_OUT<1>
MONITOR_OUT<1>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_1#
CF1_TDI
CF1_TMS
CF1_TCK
CFG_PROG_B
CFG_INIT#
FE1_DONE

CHANNEL 2

I11

FED_CHANNEL

BCLK_LVDS<2>
ICLK_LVDS<2>
READOUT_SYNC_IN<2>
FRAME_SYNC_IN<2>
CONFIG_IN<2>
MONITOR_IN<2>
+5V
5VA_NEG
1V5
3V3
GND
CF1_TDI
CF1_TMS
CF1_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD2_DATA_STREAM<0..3>
READOUT_SYNC_OUT<2>
FRAME_SYNC_OUT<2>
CONFIG_OUT<2>
MONITOR_OUT<2>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_2#
CF1_TDI
CF1_TMS
CF1_TCK
CFG_PROG_B
CFG_INIT#
FE2_DONE

CHANNEL 3

I12

FED_CHANNEL

BCLK_LVDS<3>
ICLK_LVDS<3>
READOUT_SYNC_IN<3>
FRAME_SYNC_IN<3>
CONFIG_IN<3>
MONITOR_IN<3>
+5V
5VA_NEG
1V5
3V3
GND
CF1_TDI
CF1_TMS
CF1_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD3_DATA_STREAM<0..3>
READOUT_SYNC_OUT<3>
FRAME_SYNC_OUT<3>
CONFIG_OUT<3>
MONITOR_OUT<3>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_3#
CF1_TDI
CF1_TMS
CF1_TCK
CFG_PROG_B
CFG_INIT#
FE3_DONE

CHANNEL 4

I13

FED_CHANNEL

BCLK_LVDS<4>
ICLK_LVDS<4>
READOUT_SYNC_IN<4>
FRAME_SYNC_IN<4>
CONFIG_IN<4>
MONITOR_IN<4>
+5V
5VA_NEG
1V5
3V3
GND
CF1_TDI
CF1_TMS
CF1_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD4_DATA_STREAM<0..3>
READOUT_SYNC_OUT<4>
FRAME_SYNC_OUT<4>
CONFIG_OUT<4>
MONITOR_OUT<4>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_4#
CF1_TDI
CF1_TMS
CF1_TCK
CFG_PROG_B
CFG_INIT#
FE4_DONE

CHANNEL 5

I14

FED_CHANNEL

BCLK_LVDS<5>
ICLK_LVDS<5>
READOUT_SYNC_IN<5>
FRAME_SYNC_IN<5>
CONFIG_IN<5>
MONITOR_IN<5>
+5V
5VA_NEG
1V5
3V3
GND
CF2_TDI
CF2_TMS
CF2_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD5_DATA_STREAM<0..3>
READOUT_SYNC_OUT<5>
FRAME_SYNC_OUT<5>
CONFIG_OUT<5>
MONITOR_OUT<5>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_5#
CF2_TDI
CF2_TMS
CF2_TCK
CFG_PROG_B
CFG_INIT#
FE5_DONE

CHANNEL 6

I15

FED_CHANNEL

BCLK_LVDS<6>
ICLK_LVDS<6>
READOUT_SYNC_IN<6>
FRAME_SYNC_IN<6>
CONFIG_IN<6>
MONITOR_IN<6>
+5V
5VA_NEG
1V5
3V3
GND
CF2_TDI
CF2_TMS
CF2_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD6_DATA_STREAM<0..3>
READOUT_SYNC_OUT<6>
FRAME_SYNC_OUT<6>
CONFIG_OUT<6>
MONITOR_OUT<6>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_6#
CF2_TDI
CF2_TMS
CF2_TCK
CFG_PROG_B
CFG_INIT#
FE6_DONE

CHANNEL 7

I16

FED_CHANNEL

BCLK_LVDS<7>
ICLK_LVDS<7>
READOUT_SYNC_IN<7>
FRAME_SYNC_IN<7>
CONFIG_IN<7>
MONITOR_IN<7>
+5V
5VA_NEG
1V5
3V3
GND
CF2_TDI
CF2_TMS
CF2_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD7_DATA_STREAM<0..3>
READOUT_SYNC_OUT<7>
FRAME_SYNC_OUT<7>
CONFIG_OUT<7>
MONITOR_OUT<7>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_7#
CF2_TDI
CF2_TMS
CF2_TCK
CFG_PROG_B
CFG_INIT#
FE7_DONE

CHANNEL 8

I17

FED_CHANNEL

BCLK_LVDS<8>
ICLK_LVDS<8>
READOUT_SYNC_IN<8>
FRAME_SYNC_IN<8>
CONFIG_IN<8>
MONITOR_IN<8>
+5V
5VA_NEG
1V5
3V3
GND
CF2_TDI
CF2_TMS
CF2_TCK

B_CLOCK_LVDS_IN
I_CLOCK_LVDS_IN
READOUT_SYNC_IN
FRAME_SYNC_IN
CONFIG_IN
MONITOR_IN
+5VA
5VA_NEG
1V5
3V3
GND
FE_TDI
FE_TMS
FE_TCK

DATA_STREAM<0..3>
READOUT_SYNC_OUT
FRAME_SYNC_OUT
CONFIG_OUT
MONITOR_OUT
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
FE_INT#
FE_T_CRIT#
FE_TDO
CFG_PROG_B
CFG_INIT#
FE_DONE

MOD8_DATA_STREAM<0..3>
READOUT_SYNC_OUT<8>
FRAME_SYNC_OUT<8>
CONFIG_OUT<8>
MONITOR_OUT<8>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_8#
CF2_TDI
CF2_TMS
CF2_TCK
CFG_PROG_B
CFG_INIT#
FE8_DONE

I9

FED_BACKEND

MOD1_DATA_STREAM<0..3>
MOD2_DATA_STREAM<0..3>
MOD3_DATA_STREAM<0..3>
MOD4_DATA_STREAM<0..3>
MOD5_DATA_STREAM<0..3>
MOD6_DATA_STREAM<0..3>
MOD7_DATA_STREAM<0..3>
MOD8_DATA_STREAM<0..3>
READOUT_SYNC_OUT<1..8>
FRAME_SYNC_OUT<1..8>
CONFIG_OUT<1..8>
MONITOR_OUT<1..8>
FULL_FLAG
HALF_FLAG
EMPTY_FLAG
TEMP_INT#
T_CRIT_1#
T_CRIT_2#
T_CRIT_3#
T_CRIT_4#
T_CRIT_5#
T_CRIT_6#
T_CRIT_7#
T_CRIT_8#
FE1_DONE
FE2_DONE
FE3_DONE
FE4_DONE
FE5_DONE
FE6_DONE
FE7_DONE
FE8_DONE
CF1_TD4
CF2_TDO
CFG_PROG_B
CFG_INIT#

MOD1_DATA_STREAM<0..3>
MOD2_DATA_STREAM<0..3>
MOD3_DATA_STREAM<0..3>
MOD4_DATA_STREAM<0..3>
MOD5_DATA_STREAM<0..3>
MOD6_DATA_STREAM<0..3>
MOD7_DATA_STREAM<0..3>
MOD8_DATA_STREAM<0..3>
BCLK_LVDS_OUT<1..8>
ICLK_LVDS_OUT<1..8>
READOUT_SYNC_IN<1..8>
FRAME_SYNC_IN<1..8>
CONFIG_IN<1..8>
MONITOR_IN<1..8>
+5V
5VA_NEG
3V3
1V5
GND
CF1_TDI
CF1_TMS
CF1_TCK
CF2_TDI
CF2_TMS
CF2_TCK

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	S.TAGHAVIRAD	S.TAGHAVIRAD	S.TAGHAVIRAD	

USED ON CMS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED

TOP LEVEL

A 2-TE-0070-020-01-B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020-01-B

A | 2-TE-0070-020-02-B | THIS DRAWING CONFORMS TO B.S. 3939

3V3 — C404 10N, C405 10N, C406 10N, C407 10N, C408 10N, C409 10N, C410 10N, C411 10N, C412 10N, C413 10N, C414 10N, C415 10N, C416 10N, C417 10N, C418 10N, C419 10N, C420 10N, C421 10N, C422 10N, C423 10N, C424 10N, C425 10N, C426 10N, C427 10N, C428 10N, C429 10N, C430 10N, C431 10N, C432 10N, C433 10N, C434 10N, C435 10N, C436 10N, C437 10N, C438 10N, C439 10N, C440 10N, C442 10N, C444 10N, C446 10N, C448 10N, C450 10N, C452 10N, C454 10N, C456 100N, C457 100N, C458 2U2/10V, C459 2U2/10V, C460 2U2/10V, C461 47U/10V, C462 47U/10V, C463 47U/10V, C464 220U/10V, C465 220U/10V — GND

1V5 — C439 10N, C441 10N, C443 10N, C445 10N, C447 10N, C449 10N, C451 10N, C453 10N, C455 10N, C459 10N, C461 10N, C463 10N, C465 10N, C467 10N, C469 2U2/10V — GND

BANK 0 / XC2V2000 U98 FGA -4 / BANK 1 — BODY 1 OF 7

3V3	J13	VCCO8_1	IO_L01N_0	B17	3V3
	J12	VCCO8_2	IO_L01P_0	J16	
	J11	VCCO8_3	IO_L02N_0	J15	
	H10	VCCO8_4	IO_L02P_0	J14	
	H9	VCCO8_5	IO_L03N_0/VRP_4	H18	
	B10	VCCO8_6	IO_L03P_0/VRN_4	H17	
	B7	VCCO8_7	IO_L04N_0/VREF_4	B20	
MODB_DATA_STREAM<3>	D5		IO_L04P_0	H14	CLK_LVDS_VME_B
MODB_DATA_STREAM<2>	C6		IO_L05N_0	H15	CLK_LVDS_VME
MODB_DATA_STREAM<1>	B1		IO_L05P_0	G14	CLK_LVDS_TTC_B
MODB_DATA_STREAM<0>	A2		IO_L06N_0	F14	CLK_LVDS_TTC
BNK0_VRP	D7		IO_L06P_0	E14	FRAME_SYNC_OUT<5>
BNK0_VRN	C7		IO_L07N_0	D14	FRAME_SYNC_IN<5>
CONFIG_IN<8>	B3		IO_L07P_0	A12	MOD5_DATA_STREAM<3>
CONFIG_OUT<8>	A3		IO_L08N_0	A13	MOD5_DATA_STREAM<2>
MONITOR_IN<8>	G6		IO_L08P_0	A14	MOD5_DATA_STREAM<1>
MONITOR_OUT<8>	G7		IO_L09N_0	A15	MOD5_DATA_STREAM<0>
READOUT_SYNC_IN<8>	E6		IO_L09P_0	B15	BCLK_LVDS_OUT<3>
READOUT_SYNC_OUT<8>	E7		IO_L10N_0	E15	ICLK_LVDS_OUT<3>
FRAME_SYNC_IN<8>	B4		IO_L10P_0	D15	BCLK_LVDS_OUT<4>
FRAME_SYNC_OUT<8>	A4		IO_L11N_0	E16	ICLK_LVDS_OUT<4>
MONITOR_OUT<7>	B5		IO_L11P_0/VREF_0	G15	ICLK_LVDS_OUT<7>
MONITOR_IN<7>	A5		IO_L12N_0	G16	BCLK_LVDS_OUT<5>
CONFIG_IN<7>	B6		IO_L12P_0	F16	ICLK_LVDS_OUT<5>
CONFIG_OUT<7>	A6		IO_L13N_0	A16	MOD4_DATA_STREAM<0>
FRAME_SYNC_IN<7>	A7		IO_L13P_0	A17	MOD4_DATA_STREAM<1>
FRAME_SYNC_OUT<7>	A8		IO_L14N_0	B16	MOD4_DATA_STREAM<2>
	E8		IO_L14P_0	C16	MOD4_DATA_STREAM<3>
	D8		IO_L15N_0	D16	FRAME_SYNC_IN<4>
	G8		IO_L15P_0	E16	FRAME_SYNC_OUT<4>
	F8		IO_L16N_0	C17	MONITOR_IN<4>
READOUT_SYNC_OUT<7>	C8		IO_L16P_0	D17	MONITOR_OUT<4>
READOUT_SYNC_IN<7>	B8		IO_L17N_0	H16	READOUT_SYNC_IN<4>
MOD7_DATA_STREAM<0>	D9		IO_L17P_0	G17	READOUT_SYNC_OUT<4>
MOD7_DATA_STREAM<1>	E9		IO_L18N_0	F17	CONFIG_OUT<4>
MOD7_DATA_STREAM<2>	F9		IO_L18P_0	A18	MOD3_DATA_STREAM<0>
MOD7_DATA_STREAM<3>	G9		IO_L19N_0	A19	MOD3_DATA_STREAM<1>
MOD6_DATA_STREAM<3>	B9		IO_L19P_0	B18	MOD3_DATA_STREAM<2>
MOD6_DATA_STREAM<2>	A9		IO_L20N_0	E18	MOD3_DATA_STREAM<3>
MOD6_DATA_STREAM<1>	C9		IO_L20P_0	D18	MOD3_DATA_STREAM<3>
MOD6_DATA_STREAM<0>	C10		IO_L21N_0/VREF_1	B19	FRAME_SYNC_IN<3>
CONFIG_OUT<6>	F10		IO_L21P_0	C19	FRAME_SYNC_OUT<3>
CONFIG_IN<6>	G10		IO_L22N_0	E19	MONITOR_IN<3>
MONITOR_OUT<6>	E10		IO_L22P_0	C19	MONITOR_OUT<3>
MONITOR_IN<6>	D10		IO_L23N_0	E19	READOUT_SYNC_IN<3>
READOUT_SYNC_OUT<6>	A10		IO_L23P_0	A20	READOUT_SYNC_OUT<3>
READOUT_SYNC_IN<6>	A11		IO_L24N_0	A21	CONFIG_IN<3>
FRAME_SYNC_OUT<6>	F11		IO_L24P_0	C21	CONFIG_OUT<3>
FRAME_SYNC_IN<6>	E11		IO_L25N_0	E20	MOD2_DATA_STREAM<0>
CONFIG_OUT<5>	G11		IO_L25P_0	F20	MOD2_DATA_STREAM<1>
CONFIG_IN<5>	H11		IO_L26N_0	B21	MOD2_DATA_STREAM<2>
MONITOR_OUT<5>	D11		IO_L26P_0	B22	MOD2_DATA_STREAM<3>
MONITOR_IN<5>	C11		IO_L27N_0	A22	FRAME_SYNC_IN<2>
BCLK_LVDS_OUT<3>	B11		IO_L27P_0	A23	FRAME_SYNC_OUT<2>
ICLK_LVDS_OUT<3>	B12		IO_L28N_0	C21	MONITOR_IN<2>
BCLK_LVDS_OUT<1>	G12		IO_L28P_0	D21	MONITOR_OUT<2>
ICLK_LVDS_OUT<1>	H12		IO_L29N_0/VREF_1	C20	BNK1_VRP
BCLK_LVDS_OUT<6>	F12		IO_L29P_0/VRN_1	D20	BNK1_VRN
ICLK_LVDS_OUT<6>	E12		IO_L30N_0	B24	READOUT_SYNC_IN<2>
BCLK_LVDS_OUT<8>	D12		IO_L30P_0	A25	READOUT_SYNC_OUT<2>
ICLK_LVDS_OUT<8>	C12		IO_L31N_0	B23	CONFIG_OUT<2>
READOUT_SYNC_OUT<5>	G13		IO_L31P_0/GCLK15	B24	CONFIG_IN<2>
READOUT_SYNC_IN<5>	H13		IO_L32N_0/GCLK14		
TP73 1 BE_TP2	F13		IO_L32P_0/GCLK13		
TP74 1 BE_TP3	E13		IO_L01N_0/GCLK7P		
TP75 1 BE_TP2	D13		IO_L01P_0/GCLK6S		
TP76 1 BE_TP1	C13		IO_L16N_0/GCLK5P		
			IO_L16P_0/GCLK4S		

3V3 — R182 4K7, R183 4K7, R184 4K7, R185 4K7

TP4 1 BE_TP5

BANK 2 / XC2V2000 U98 FGA -4 / BANK 3 — BODY 2 OF 7

3V3	N18	VCCO2_1	IO_L01N_2	B26	MOD1_DATA_STREAM<0>
	M18	VCCO2_2	IO_L01P_2	G26	MOD1_DATA_STREAM<1>
	L18	VCCO2_3	IO_L02N_2/A0/D24	G20	BNK2_VRP
	K25	VCCO2_4	IO_L02P_2/A1/D25	H20	BNK2_VRN
	K19	VCCO2_5	IO_L03N_2/A2/D26	C25	MOD1_DATA_STREAM<2>
	J19	VCCO2_6	IO_L03P_2/A3/D27	D25	MOD1_DATA_STREAM<3>
	G25	VCCO2_7	IO_L04N_2	F23	FRAME_SYNC_OUT<1>
MOD1_DATA_STREAM<0>	B26		IO_L04P_2	E23	FRAME_SYNC_IN<1>
MOD1_DATA_STREAM<1>	G26		IO_L05N_2	G21	READOUT_SYNC_OUT<1>
BNK2_VRP	G20		IO_L05P_2	G22	READOUT_SYNC_IN<1>
BNK2_VRN	H20		IO_L06N_2	D26	MONITOR_OUT<1>
MOD1_DATA_STREAM<2>	C25		IO_L06P_2	E26	MONITOR_IN<1>
MOD1_DATA_STREAM<3>	D25		IO_L07N_2	F23	CONFIG_OUT<1>
FRAME_SYNC_OUT<1>	E23		IO_L07P_2	F24	CONFIG_IN<1>
FRAME_SYNC_IN<1>	F24		IO_L08N_2	F22	EMPTY_FLAG
READOUT_SYNC_OUT<1>	G21		IO_L08P_2	F25	HALF_FLAG
READOUT_SYNC_IN<1>	G22		IO_L09N_2	H22	FULL_FLAG
MONITOR_OUT<1>	D26		IO_L09P_2	H21	BE_TP5
MONITOR_IN<1>	E26		IO_L10N_2	G23	
CONFIG_OUT<1>	F23		IO_L10P_2	G24	
CONFIG_IN<1>	F24		IO_L11N_2	F26	TEMP_WARN
EMPTY_FLAG	E22		IO_L11P_2	G25	FLT
HALF_FLAG	F25		IO_L12N_2	H23	EMU
FULL_FLAG	H22		IO_L12P_2	H24	FSYNC
BE_TP5	H21		IO_L13N_2	J21	DPROCESS
	G23		IO_L13P_2	J20	TRANSFER
	G24		IO_L14N_2	H25	READOUT
TEMP_WARN	F26		IO_L14P_2	H26	T_BUSY
FLT	G25		IO_L15N_2	J22	TTC_ERROR
EMU	H23		IO_L15P_2/A4/D28	J23	DAQ_HALT
FSYNC	H24		IO_L16N_2/A5/D29	K21	
DPROCESS	J21		IO_L16P_2/A6/D30	K22	
TRANSFER	J20		IO_L17N_2/A7/D31	K20	
READOUT	H25		IO_L17P_2	L20	RST
T_BUSY	H26		IO_L18N_2	J24	TTC_RST_FRM_VME
TTC_ERROR	J22		IO_L18P_2	J25	TTC_READY_TO_VME
DAQ_HALT	J23		IO_L19N_2	K23	LOCAL_VME_SPARE<4>
	K21		IO_L19P_2	K24	LOCAL_VME_SPARE<3>
RST	L20		IO_L20N_2/A8/D32	J26	LOCAL_VME_SPARE<2>
TTC_RST_FRM_VME	J24		IO_L20P_2/A9/D33	K26	LOCAL_VME_SPARE<1>
TTC_READY_TO_VME	J25		IO_L21N_2	L22	VME_CMND_OUT
LOCAL_VME_SPARE<4>	K23		IO_L21P_2	L21	VME_CMND_IN
LOCAL_VME_SPARE<3>	K24		IO_L22N_2	L25	VME_THROTTLE
LOCAL_VME_SPARE<2>	J26		IO_L22P_2	L26	DATA_TO_VME_VALID
LOCAL_VME_SPARE<1>	K26		IO_L23N_2	L19	DATA_OUT_TO_VME<31>
VME_CMND_OUT	L22		IO_L23P_2	M19	DATA_OUT_TO_VME<30>
VME_CMND_IN	L21		IO_L24N_2	L23	DATA_OUT_TO_VME<29>
VME_THROTTLE	L25		IO_L24P_2	L24	DATA_OUT_TO_VME<28>
DATA_TO_VME_VALID	L26		IO_L25N_2	M22	DATA_OUT_TO_VME<27>
DATA_OUT_TO_VME<31>	L19		IO_L25P_2	M21	DATA_OUT_TO_VME<26>
DATA_OUT_TO_VME<30>	M19		IO_L26N_2/A10/D34	M23	DATA_OUT_TO_VME<25>
DATA_OUT_TO_VME<29>	L23		IO_L26P_2/A11/D35	M24	DATA_OUT_TO_VME<24>
DATA_OUT_TO_VME<28>	L24		IO_L27N_2/A12/D36	M25	DATA_OUT_TO_VME<23>
DATA_OUT_TO_VME<27>	M22		IO_L27P_2/A13/D37	M26	DATA_OUT_TO_VME<22>
DATA_OUT_TO_VME<26>	M21		IO_L28N_2/A14/D38	N22	DATA_OUT_TO_VME<21>
DATA_OUT_TO_VME<25>	M23		IO_L28P_2/A15/D39	M20	DATA_OUT_TO_VME<20>
DATA_OUT_TO_VME<24>	M24		IO_L29N_2/A16/D40	N20	DATA_OUT_TO_VME<19>
DATA_OUT_TO_VME<23>	M25		IO_L29P_2/A17/D41	N21	DATA_OUT_TO_VME<18>
DATA_OUT_TO_VME<22>	M26		IO_L30N_2/A18/D42	N24	DATA_OUT_TO_VME<17>
DATA_OUT_TO_VME<21>	M20		IO_L30P_2/A19/D43	N23	DATA_OUT_TO_VME<16>
DATA_OUT_TO_VME<20>	N20		IO_L31N_2/A20/D44		
DATA_OUT_TO_VME<19>	N22		IO_L31P_2/A21/D45		
DATA_OUT_TO_VME<18>	N21		IO_L32N_2/A22/D46		
DATA_OUT_TO_VME<17>	N24		IO_L32P_2/A23/D47		
DATA_OUT_TO_VME<16>	N23		IO_L01N_3	Y25	
			IO_L01P_3	AA22	SLINK_UD<15>

3V3 — Y25, U19, U5, U19, T18, R18, P18

BANK 4 / XC2V2000 U98 FGA -4 / BANK 5 — BODY 3 OF 7

3V3	AE20	VCCO4_1	IO_L01N_4/DOUT	AE10	3V3
	AE17	VCCO4_2	IO_L01P_4/INIT_B	AE7	
	W18	VCCO4_3	IO_L02N_4/D0	W10	
	W17	VCCO4_4	IO_L02P_4/D1	W9	
	V16	VCCO4_5	IO_L03N_4/D2/ALT_VRP_4	V13	
	V15	VCCO4_6	IO_L03P_4/D3/ALT_VRN_4	V12	
	V14	VCCO4_7	IO_L04N_4/VREF_4	V11	
BE_J2_SPARE<1>			IO_L04P_4		
CFG_INIT#_LK2842-C	AD21		IO_L05N_4/VRP_4	AC13	TTC_CLK40
	AC21		IO_L05P_4/VRN_4	AB13	TTC_DOUTSTR
SLINK_UD<16>	Y20		IO_L06N_4/D4	AA13	TTS_J0_READY_B
SLINK_UD<17>	Y19		IO_L06P_4/D5	Y13	TTS_J0_READY
SLINK_UD<18>	AA20		IO_L07N_4/D6	W13	TTS_J0_BUSY_B
SLINK_UD<19>	AB20		IO_L07P_4/D7	W12	TTS_J0_BUSY
SLINK_UD<20>	AC22		IO_L08N_4/VREF_4	AF15	TTS_J0_WARN_OVRFLW_B
SLINK_UD<21>	AE21		IO_L08P_4	AF14	TTS_J0_WARN_OVRFLW
BNK4_VRP	AE26		IO_L09N_4/VRP_4	AF13	TTS_J0_OUT_OF_SYNC_B
BNK4_VRN	AF25		IO_L09P_4/VRN_4	AF12	TTS_J0_OUT_OF_SYNC
SLINK_UD<22>	W20		IO_L10N_4	AE12	TEST_TRIG_B
SLINK_UD<23>	Y21		IO_L10P_4	AD12	TEST_TRIG
SLINK_UD<24>	AF24		IO_L11N_4	AC12	BE_J0_SPARE<0>
SLINK_UD<25>	AF24		IO_L11P_4	AB12	BE_J0_SPARE<1>
SLINK_UD<26>	AF23		IO_L21N_4	AA12	BE_J0_SPARE<2>
SLINK_UD<27>	AF23		IO_L21P_4/VREF_4	Y12	BE_J0_SPARE<3>
SLINK_UD<28>	AF22		IO_L22N_4	AF11	TTC_DB_ERR_STR
SLINK_UD<29>	AF22		IO_L22P_4	AF10	TTC_SIN_ERR_STR
SLINK_UD<30>	AF21		IO_L24N_4	AE11	TTC_BRCST_STR<1>
SLINK_UD<31>	AF20		IO_L24P_4	AD11	TTC_BRCST_STR<2>
	AA19		IO_L25N_4	AC11	TTC_READY
	AB19		IO_L25P_4	AB11	TTC_EVT_CNT_RST
	AD20		IO_L27N_4	W11	TTC_BCNT_RST
	AC20		IO_L27P_4/VREF_4	Y10	TTC_L1_ACCEPT
	AC19		IO_L28N_4	Y11	TTC_BRDCST<2>
	AD19		IO_L28P_4	AA11	TTC_BRDCST<3>
SLINK_UD<32>	AC19		IO_L29N_4	AF9	TTC_BRDCST<4>
SLINK_UD<33>	AF19		IO_L29P_4	AF8	TTC_BRDCST<5>
SLINK_UD<34>	AA18		IO_L31N_4	AE9	TTC_BRDCST<6>
SLINK_UD<35>	AB18		IO_L31P_4/VREF_4	AD9	TTC_BRDCST<7>
SLINK_UD<36>	Y18		IO_L32N_4	AB10	TTC_SERIAL_B
SLINK_UD<37>	Y17		IO_L32P_4	AA10	TTC_RESET_B
SLINK_UD<38>	AC18		IO_L34N_4	AD10	TTC_SCL
SLINK_UD<39>	AD18		IO_L34P_4	AC10	TTC_SDA
SLINK_UD<40>	AE18		IO_L35N_4	AE8	TTC_CLKLIACCEPT
SLINK_UD<41>	AF18		IO_L35P_4	AF7	TTS_J2_READY
SLINK_UD<42>	AA17		NC_L26N_5	AD8	
SLINK_UD<43>	AB17		NC_L26P_5	AC8	
SLINK_UD<44>	AC17		NC_L27N_5/VREF_5	AB9	
SLINK_UD<45>	AD17		NC_L27P_5	AC9	
SLINK_UD<46>	AF17		NC_L29N_5	AA9	
SLINK_UD<47>	AF16		NC_L29P_5	Y9	
SLINK_UD<48>	AB16		IO_L34N_5	AF6	TTS_J2_BUSY
SLINK_UD<49>	AC16		IO_L34P_5	AE6	TTS_J2_WARN_OVRFLW
SLINK_UD<50>	AA16		IO_L35N_5	AB8	TTS_J2_OUT_OF_SYNC
SLINK_UD<51>	Y16		IO_L35P_5	AA8	TTC_DO_0
SLINK_UD<52>	AD16		IO_L36N_5/VREF_5	AC7	TTC_DO_1
SLINK_UD<53>	AE16		IO_L36P_5	AD7	TTC_DO_2
SLINK_UD<54>	Y15		IO_L37N_5	AF5	TTC_DO_3
SLINK_UD<55>	AA15		IO_L37P_5	AE5	DOUT0
SLINK_UD<56>	W15		IO_L38N_5	AF4	DOUT1
SLINK_UD<57>	W15		IO_L38P_5	AE4	DOUT2
SLINK_UD<58>	AB15		IO_L39N_5/VRP_5	AF3	BNK5_VRP
SLINK_UD<59>	AC15		IO_L39P_5/VRN_5	AE3	BNK5_VRN
SLINK_UD<60>	AD15		IO_L40N_5	Y8	DOUT3
SLINK_UD<61>	AE15		IO_L40P_5/VREF_5	Y7	DOUT4
SLINK_UCLK_B	W14		IO_L41N_5/D24/ALT_VRP_5	AB7	DOUT5
SLINK_UCLK	Y14		IO_L41P_5/D25/ALT_VRN_5	AA7	DOUT6
SLINK_UD<62>	AA14		IO_L42N_5/D26	AD6	DOUT7
SLINK_UD<63>	AB14		IO_L42P_5/D27	AC6	TEMP_INT#
TTC_CLK40_DES1	AC14		IO_L43N_5/RDWR_B	AB6	BE_SYSCLK
TTC_CLK40_DES2	AD14		IO_L43P_5/CS_B	AC5	BE_SMBDATA

GND — TP76

BANK 6 / XC2V2000 U98 FGA -4 / BANK 7 — BODY 4 OF 7

1V5	Y2	VCCO6_1	IO_L01P_6	N9	1V5
	V8	VCCO6_2	IO_L01N_6	M9	
	U8	VCCO6_3	IO_L02P_6/VRN_6	L9	
	U2	VCCO6_4	IO_L02N_6/VRP_6	K8	
	T9	VCCO6_5	IO_L03P_6	K2	
	R9	VCCO6_6	IO_L03N_6/VREF_6	J8	
	P9	VCCO6_7	IO_L04P_6	G2	
QDR2_DATA<17>	AF2		IO_L04N_6	P1	QDR_CLK_K
QDR2_DATA<16>	AE1		IO_L05P_6	N1	QDR_CLK_K#
BNK6_VRN	AB4		IO_L05N_6	M4	QDR_ADDR<1>
BNK6_VRP	AB3		IO_L06P_6/VRN_6	N4	QDR_ADDR<10>
QDR2_DATA<15>	AD2		IO_L06N_6/VRP_6	N5	QDR_READY
BNK6_VREF	AD1		IO_L07P_6	N6	BNK7_VREF
QDR2_DATA<14>	AC2		IO_L07N_6/VREF_6	N7	QDR_ADDR<9>
QDR2_DATA<13>	AC1		IO_L08P_6	P8	QDR_ADDR<8>
QDR2_DATA<12>	AB2		IO_L08N_6	N8	QDR_ADDR<7>
QDR2_DATA<11>	AB1		IO_L09P_6	M1	QDR_ADDR<6>
QDR2_DATA<10>	AA4		IO_L09N_6	M2	QDR_ADDR<5>
QDR2_DATA<9>	AA3		IO_L10P_6	M5	QDR_ADDR<4>
QDR2_DATA<8>	AA2		IO_L10N_6	M6	QDR_ADDR<3>
BNK6_VREF	Y5		IO_L11P_6	M3	BNK7_VREF
QDR2_DATA<7>	W6		IO_L11N_6/VREF_6	M4	QDR_ADDR<2>
QDR2_DATA<6>	W7		IO_L12P_6	M7	QDR_ADDR<1>
QDR2_DATA<5>	AA5		IO_L12N_6	M8	QDR2_Q<17>
QDR2_DATA<4>	AA1		IO_L13P_6	L1	QDR2_Q<16>
	Y4		IO_L13N_6	L2	QDR2_Q<15>
	Y3		NC_L25P_6	L5	QDR2_Q<14>
QDR2_DATA<3>	W5		NC_L25N_6	L6	QDR2_Q<13>
QDR2_DATA<2>	W4		IO_L14P_6	L3	BNK7_VREF
QDR2_DATA<1>	W2		IO_L14N_6	L4	QDR2_Q<12>
BNK6_VREF	W3		IO_L15P_6	K1	QDR2_Q<11>
QDR2_DATA<0>	Y1		IO_L15N_6/VREF_6	J1	QDR2_Q<10>
QDR1_DATA<17>	W1		IO_L16P_6	K3	QDR2_Q<9>
QDR1_DATA<16>	V5		IO_L16N_6	K4	QDR2_Q<8>
QDR1_DATA<15>	V7		IO_L17P_6	K5	QDR2_Q<7>
QDR1_DATA<14>	V5		IO_L17N_6	K6	QDR2_Q<6>
QDR1_DATA<13>	V4		IO_L18P_6	L8	BNK7_VREF
QDR1_DATA<12>	V3		IO_L18N_6	L7	QDR2_Q<5>
BNK6_VREF	V2		IO_L19P_6	J2	QDR2_Q<4>
QDR1_DATA<11>	V1		IO_L19N_6/VREF_6	H1	QDR2_Q<3>
QDR1_DATA<10>	T2		IO_L20P_6	J3	QDR2_Q<2>
QDR1_DATA<9>	U7		IO_L20N_6	J4	QDR2_Q<1>
QDR1_DATA<8>	T7		IO_L21P_6	J5	QDR2_Q<0>
QDR1_DATA<7>	U4		IO_L21N_6	J6	QDR1_Q<17>
QDR1_DATA<6>	U3		IO_L22P_6	H5	BNK7_VREF
QDR1_DATA<5>	U6		IO_L22N_6/VREF_6	H4	QDR1_Q<16>
BNK6_VREF	U5		IO_L23P_6	K7	QDR1_Q<15>
QDR1_DATA<4>	T5		IO_L23N_6	J7	QDR1_Q<14>
QDR1_DATA<3>	T6		NC_L25P_7	H2	
QDR1_DATA<2>	T8		NC_L25N_7	H3	
QDR1_DATA<1>	R8		IO_L24P_7	G1	QDR1_Q<13>
QDR1_DATA<0>	T2		IO_L24N_7	F1	QDR1_Q<12>
QDR_WRITE#	T1		IO_L23N_7	G4	QDR1_Q<11>
QDR_READ#	T4		IO_L23P_7/VREF_7	F3	BNK7_VREF
BNK6_VREF	T3		IO_L21N_7	F2	QDR1_Q<9>
QDR_BW#	R6		IO_L21P_7	H6	QDR1_Q<8>
QDR_ADDR<19>	R5		IO_L19N_7	H7	QDR1_Q<7>
QDR_ADDR<18>	R4		IO_L19P_7	E1	QDR1_Q<6>
QDR_ADDR<17>	R3		IO_L18N_7	E2	QDR1_Q<5>
QDR_ADDR<16>	R2		IO_L18P_7	D1	QDR1_Q<4>
QDR_ADDR<15>	R1		IO_L17N_7	D2	QDR1_Q<3>
QDR_ADDR<14>	P7		IO_L17P_7/VREF_7	C1	BNK7_VREF
BNK6_VREF	P6		IO_L16N_7	C2	QDR1_Q<2>
QDR_ADDR<13>	P5		IO_L16P_7/VRN_7	E3	BNK7_VRN
QDR_ADDR<12>	P4		IO_L15N_7/VRP_7	E4	BNK7_VRP
QDR_CLK_C	P3		IO_L15P_7	G5	QDR1_Q<1>
QDR_CLK_C#			IO_L14N_7	F4	QDR1_Q<0>

BNK0_VRP / BNK0_VRN / BNK1_VRP / BNK1_VRN / BNK2_VRP / BNK2_VRN / BNK3_VRP / BNK3_VRN / BNK4_VRP / BNK4_VRN / BNK5_VRP / BNK5_VRN / BNK6_VRP / BNK6_VRN / BNK7_VRP / BNK7_VRN

R186 56R, R187 56R, R188 56R, R189 56R, R190 56R, R191 56R, R192 56R, R193 56R, R194 56R, R195 56R, R196 56R, R197 56R, R198 56R, R199 56R, R200 56R, R201 56R

GND, 3V3, 1V5

R185 1K0 5% 0402 — D59 RED — GND

DATA_OUT_TO_VME<15..0>

DATA_OUT_TO_VME<15>	N26	IO_L99N_3	
DATA_OUT_TO_VME<14>	P26	IO_L99P_3	
DATA_OUT_TO_VME<13>	P23	IO_L98N_3	
DATA_OUT_TO_VME<12>	P22	IO_L98P_3	
DATA_OUT_TO_VME<11>	P19	IO_L93N_3/VREF_3	
DATA_OUT_TO_VME<10>	N19	IO_L93P_3	
DATA_OUT_TO_VME<9>	P21	IO_L91N_3	
DATA_OUT_TO_VME<8>	P20	IO_L91P_3	
DATA_OUT_TO_VME<7>	R26	IO_L78N_3	
DATA_OUT_TO_VME<6>	R25	IO_L78P_3	
DATA_OUT_TO_VME<5>	R20	IO_L76N_3	
DATA_OUT_TO_VME<4>	R19	IO_L76P_3	
DATA_OUT_TO_VME<3>	R24	IO_L75N_3/VREF_3	
DATA_OUT_TO_VME<2>	R23	IO_L75P_3	
DATA_OUT_TO_VME<1>	R22	IO_L73N_3	
DATA_OUT_TO_VME<0>	R21	IO_L73P_3	
LOCAL_VME_SPARE<5>	T26	IO_L72N_3	
LOCAL_VME_SPARE<6>	T25	IO_L72P_3	
BE_LED	T20	IO_L70N_3	
SLINK_LDOWN#	T19	IO_L70P_3	
SLINK_LSF<0>	T24	IO_L69N_3/VREF_3	
SLINK_LSF<1>	T23	IO_L69P_3	
SLINK_LSF<2>	T22	IO_L67N_3	
SLINK_LSF<3>	T21	IO_L67P_3	
SLINK_LFF#	U26	IO_L54N_3	
BE_J2_SPARE<0>	U25	IO_L54P_3	
SLINK_LRL<0>	U24	IO_L52N_3	
SLINK_LRL<1>	U23	IO_L52P_3	
SLINK_LRL<2>	U22	IO_L51N_3/VREF_3	
SLINK_LRL<3>	U21	IO_L51P_3	
SLINK_USF<3>	V26	IO_L49N_3	
SLINK_USF<2>	V25	IO_L49P_3	
SLINK_USF<1>	V24	IO_L48N_3	
SLINK_USF<0>	V23	IO_L48P_3	
SLINK_UWEN#	W26	IO_L46N_3	
SLINK_UCNTL#	W25	IO_L46P_3	
SLINK_UTEST#	V20	IO_L45N_3/VREF_3	
SLINK_URESET#	V20	IO_L45P_3	
SLINK_UDW0	W24	IO_L43N_3	
SLINK_UDW1	W24	IO_L43P_3	
	V21	NC_L25N_3	
SLINK_UD<0>	AB26	NC_L25P_3	
SLINK_UD<1>	AB25	IO_L24N_3	
SLINK_UD<2>	Y24	IO_L24P_3	
SLINK_UD<3>	Y23	IO_L22N_3	
SLINK_UD<4>	W22	IO_L22P_3	
SLINK_UD<5>	W23	IO_L21N_3/VREF_3	
SLINK_UD<6>	AB26	IO_L21P_3	
SLINK_UD<7>	AB25	IO_L19N_3	
SLINK_UD<8>	AC26	IO_L19P_3	
SLINK_UD<9>	AC25	IO_L18N_3	
SLINK_UD<10>	AD26	IO_L18P_3	
SLINK_UD<11>	AD25	IO_L17N_3	
SLINK_UD<12>	AB24	IO_L17P_3/VREF_3	
SLINK_UD<13>	AB23	IO_L16N_3	
SLINK_UD<14>	AB24	IO_L16P_3	
SLINK_UD<15>	AB23	IO_L01N_3	
	Y22	IO_L01P_3	
	AA22		

BNK6_VREF / BNK7_VREF

R202 4K7 1% 0402 — BNK6_VREF — C5 10N — GND — C456 100N +/-15% — 1V5

R203 5K6 1% 0402 — BNK7_VREF — C5 10N — GND — C457 100N +/-15% — 1V5

R204 4K7 1% 0402 — BNK6_VREF — C5 10N — GND — C456 100N +/-15% — 1V5

R205 5K6 1% 0402 — BNK7_VREF — C5 10N — GND — C457 100N +/-15% — 1V5

MOD8_DATA_STREAM<0..3>, MOD7_DATA_STREAM<0..3>, MOD6_DATA_STREAM<0..3>, MOD5_DATA_STREAM<0..3>, MOD4_DATA_STREAM<0..3>, MOD3_DATA_STREAM<0..3>, MOD2_DATA_STREAM<0..3>, MOD1_DATA_STREAM<0..3>

IN

EMPTY_FLAG, HALF_FLAG, FULL_FLAG, TEMP_INT#

IN

CONFIG_IN<1..8>, CONFIG_OUT<1..8>, MONITOR_IN<1..8>, MONITOR_OUT<1..8>, READOUT_SYNC_IN<1..8>, READOUT_SYNC_OUT<1..8>, FRAME_SYNC_IN<1..8>, FRAME_SYNC_OUT<1..8>

IN → OUT

BCLK_LVDS_OUT<1..8>, ICLK_LVDS_OUT<1..8>

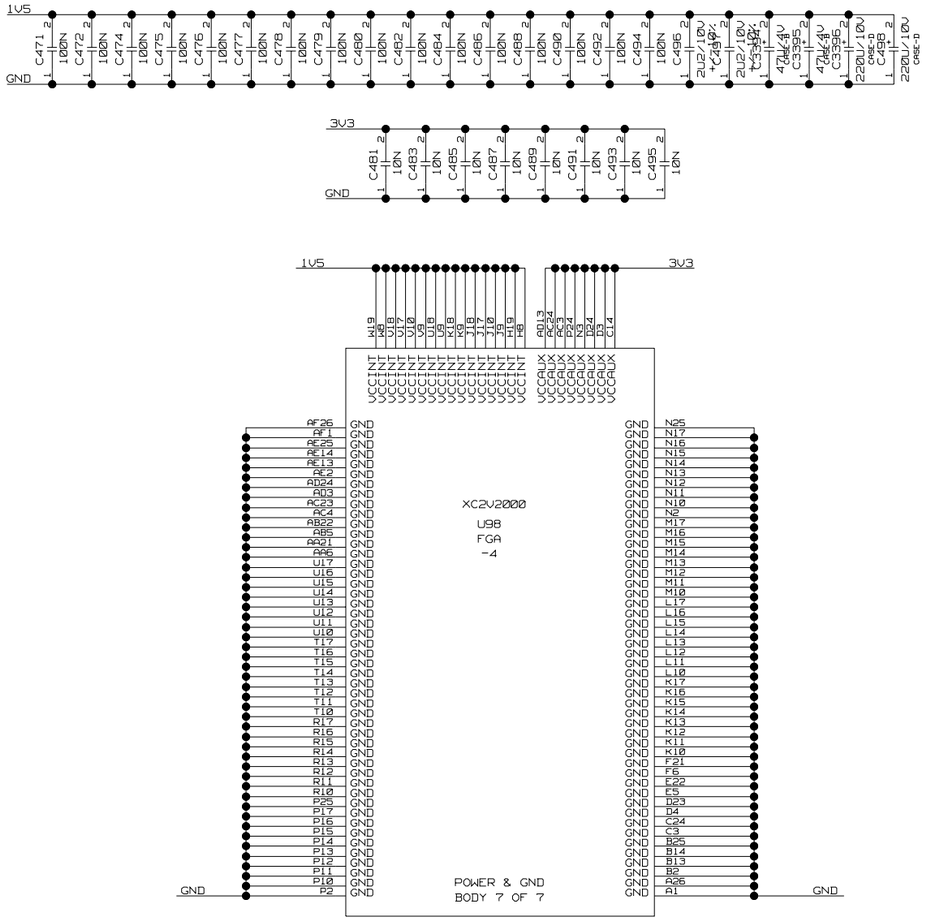
OUT

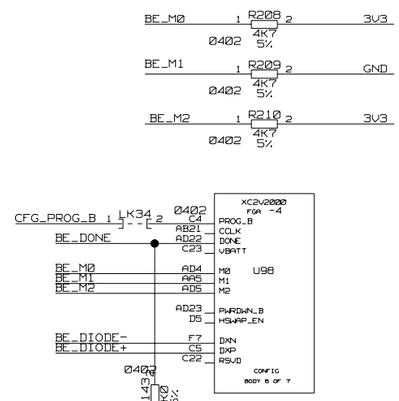
CLK_LVDS_VME_B, CLK_LVDS_VME

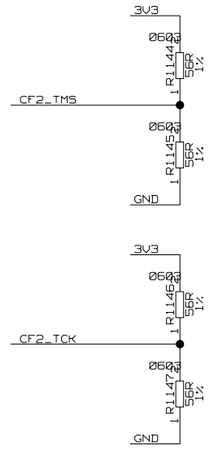
R5 100R 0402

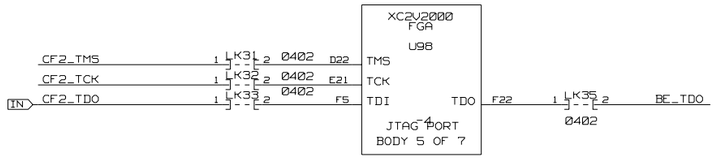
PLACE RESISTOR AT PINS UNDER U98.

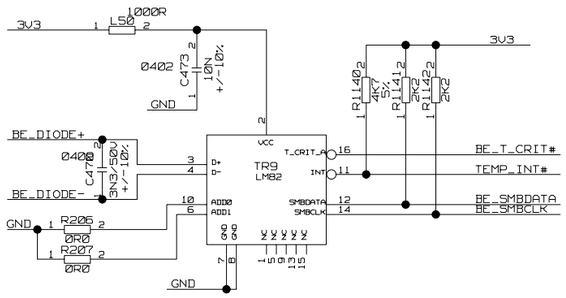
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12











ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

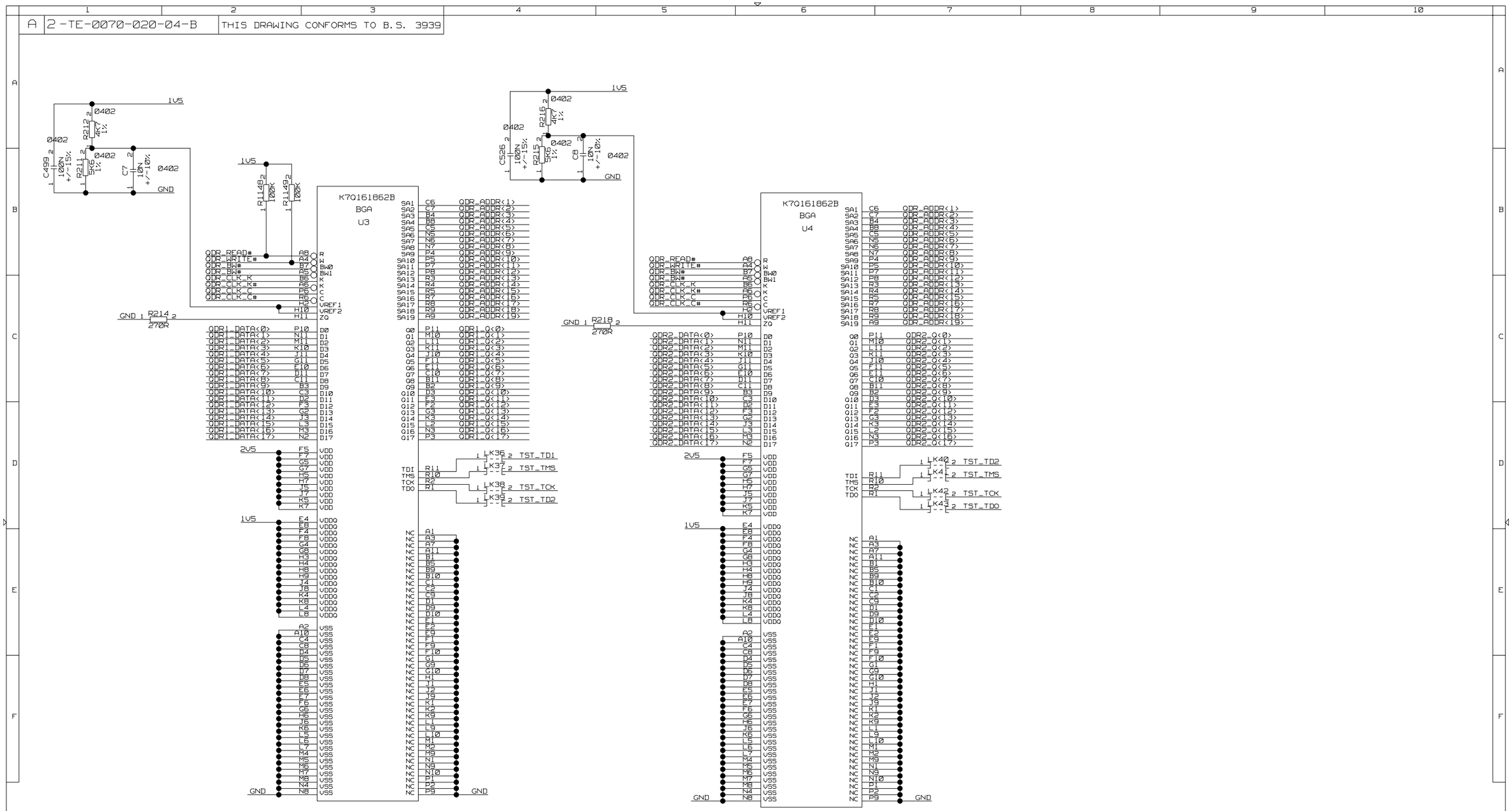
PC3205M CIRCUIT

CMS TRACKER FED
BACK END FPGA

A2-TE-0070-020-03-B

TOTAL NO. OF SHEETS 95

A2 -TE-0070-020-03-B



ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON: CMS

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CCLRC
COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE
PC3205M CIRCUIT
CMS TRACKER FED
QDR MEMORY

A 2-TE-0070-020-04-B

TOTAL NO. OF SHEETS 95

A 2 -TE-0070-020-04-B

A	2 -TE-0070-020-05-B	THIS DRAWING CONFORMS TO B.S. 3939

ID0 3V3 R1156 100K PL25 1A; DOUT0 2A; GND R1157 100K 3A
ID1 3V3 R1154 100K PL24 1A; DOUT1 2A; GND R1155 100K 3A
ID2 3V3 R1152 100K PL23 1A; DOUT2 2A; GND R1153 100K 3A
ID3 3V3 R1150 100K PL22 1A; DOUT3 2A; GND R1151 100K 3A
ID4 3V3 R1158 100K PL26 1A; DOUT4 2A; GND R1159 100K 3A
ID5 3V3 R1160 100K PL27 1A; DOUT5 2A; GND R1161 100K 3A
ID6 3V3 R1162 100K PL28 1A; DOUT6 2A; GND R1163 100K 3A
ID7 3V3 R1164 100K PL29 1A; DOUT7 2A; GND R1165 100K 3A
ID8 3V3 R1166 100K PL30 1A; SUBADDR0 2A; GND R1167 100K 3A
ID9 3V3 R1168 100K PL31 1A; SUBADDR1 2A; GND R1169 100K 3A
ID10 3V3 R1170 100K PL32 1A; SUBADDR2 2A; GND R1171 100K 3A
ID11 3V3 R1172 100K PL33 1A; SUBADDR3 2A; GND R1173 100K 3A
ID12 3V3 R1174 100K PL34 1A; SUBADDR4 2A; GND R1175 100K 3A
ID13 3V3 R1176 100K PL35 1A; SUBADDR5 2A; GND R1177 100K 3A
NM0 3V3 R1178 100K PL36 1A; SUBADDR6 2A; GND R1179 100K 3A
NM1 3V3 R1180 100K PL37 1A; SUBADDR7 2A; GND R1181 100K 3A

NM0 AND NM1 SHOULD BE SET TO GND
FOR NORMAL OPERATION

CONNECT NC PINS TO GND

U102 TRR-1843-000 DOUT DOUT VCC GND PWD

DIRECT SIGNAL PATH: SHORT,
SYMMETRICAL & CLOSE TOGETHER

C553 10N; C554 10N; C562 100N; C563 100N; R224 100R 1% 0402

+5V; GND; C563 10U 16V +/-10%; C564 100N +/-10%

OPTIMALLY PLACE FOR DIFFERENTIAL

3V3; GND; C555 2U2/10V +/-10%; C559 2U2/10V +/-10%; C564 100N; C567 100N; C571 100N; C573 100N; C575 100N; C577 100N; C578 100N

3V3; GND; C556 2U2/10V +/-10%; C562 100N; C565 100N; C568 100N

3V3; GND; CASE-C; C558 47U/10V +/-10%; L51 1000R Ferrite; C570 2U2/10V +/-10%; C572 100N; C574 100N; C576 100N

3V3; GND; C557 2U2/10V +/-10%; C561 100N; C566 100N; C569 100N

3V3; R220 2K2; R221 2K2; TTC_SCL; TTC_SDA

U103 TTCRX BGA

D1	D_VDD_I/O	
M1	D_VDD_I/O	
M4	D_VDD_I/O	
H9	D_VDD_I/O	
E12	D_VDD_I/O	
B8	D_VDD_I/O	
A5	D_VDD_I/O	
E3	D_VDD_CORE	
K7	D_VDD_CORE	
J12	D_VDD_CORE	
F5	A_VDD	
G3	A_VDD	
G4	A_VDD	
H12	D_VDD_C	
G9	D_VDD_C	
G10	D_VDD_C	
C2	RESET_B	TTC_RESET_B; GND R1182 4K7 5%; GND R6 4K7 5%
C1	PROMD	
F1	IN	
G1	IN_B	
H3	SCL	TTC_SCL
J2	SDA	TTC_SDA
H11	CLOCK40	TTC_CLK40
G12	CLOCK40DES1	TTC_CLK40_DES1
F12	CLOCK40DES2	TTC_CLK40_DES2
F8	CLOCK1ACCEPT	TTC_CLK1ACCEPT; TP80; TP79; TP78; TP77
G2	G_GND	GND
F4	D_GND_I/O	
G5	D_GND_I/O	
E1	D_GND_CORE	
K5	GND_I/O	
H10	GND_I/O	
E10	GND_I/O	
C8	GND_I/O	
D6	GND_I/O	
M8	GND_CORE1	
F7	GND_CORE2	
G8	D_GND_C1	
G11	D_GND_C2	
E11	D_GND_C3	
F2	GND	
M2	GND	

BODY 1 OF 2

E5	PROMCLK	
D3	PROMRESET	
D2	TTCREADY	TTC_READY; R227 1K0 5% 0402; DS11 RED; GND; R225 100K 5% 0402
K4	SERIAL_B_CHANNEL	TTC_SERIAL_B
H6	BCNT<11>	TTC_BCNT_11; TP84
L4	BCNT<10>	TTC_BCNT_10; TP86
L5	BCNT<9>	TTC_BCNT_9; TP89
M5	BCNT<8>	TTC_BCNT_8; TP92
J5	BCNT<7>	TTC_BCNT_7; TP94
J6	BCNT<6>	TTC_BCNT_6; TP95
L6	BCNT<5>	TTC_BCNT_5; TP96
M6	BCNT<4>	TTC_BCNT_4; TP97
K6	BCNT<3>	TTC_BCNT_3; TP98
G7	BCNT<2>	TTC_BCNT_2; TP99
M7	BCNT<1>	TTC_BCNT_1; TP100
L7	BCNT<0>	TTC_BCNT_0
L8	BCNTSTR	TTC_BCNTSTR; TP85
J7	EVCNTHSTR	TTC_EVCNTHSTR; TP87
K8	EVCNTLSTR	TTC_EVCNTLSTR
M9	BCNTRES	TTC_BCNT_RST
L9	EVCNTRES	TTC_EVT_CNT_RST
J8	L1ACCEPT	TTC_L1_ACCEPT
K12	BRCSTSTR2	TTC_BRCST_STR<2>
D10	BRCSTSTR1	TTC_BRCST_STR<1>
E9	SINERRSTR	TTC_SIN_ERR_STR
C12	DBERRSTR	TTC_DB_ERR_STR
F6	SUBADDR7	
D8	SUBADDR6	
A8	SUBADDR5	
C9	SUBADDR4	
A9	SUBADDR3	
B9	SUBADDR2	
E7	SUBADDR1	
E8	SUBADDR0	
K9	BRCST<7>	TTC_BRDCST<7>
K11	BRCST<6>	TTC_BRDCST<6>
J10	BRCST<5>	TTC_BRDCST<5>
J11	BRCST<4>	TTC_BRDCST<4>
D11	BRCST<3>	TTC_BRDCST<3>
D12	BRCST<2>	TTC_BRDCST<2>
D7	DQ<3>	TTC_DQ_3
C7	DQ<2>	TTC_DQ_2
A7	DQ<1>	TTC_DQ_1
B7	DQ<0>	TTC_DQ_0
A6	DOUTSTR	TTC_DOUTSTR
C4	DOUT<7>	DOUT7
B4	DOUT<6>	DOUT6
A4	DOUT<5>	DOUT5
D5	DOUT<4>	DOUT4
C5	DOUT<3>	DOUT3
B5	DOUT<2>	DOUT2
C6	DOUT<1>	DOUT1
B6	DOUT<0>	DOUT0

BGA CERN

DO NOT FIT R1183 0402 0R0 5%

U103 TTCRX BGA

H4	JTAGTDI	TEST_TDI; LK44
J3	JTAGTMS	TEST_TMS; LK45
K1	JTAGTCK	TEST_TCK; LK46
M2	JTAGTRST_B	TEST_TRST_B; C1
J1	JTAGTDO	LK285; TEST_TDI

BODY 2 OF 2 BGA CERN

GND; R225 100K 5% 0402

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

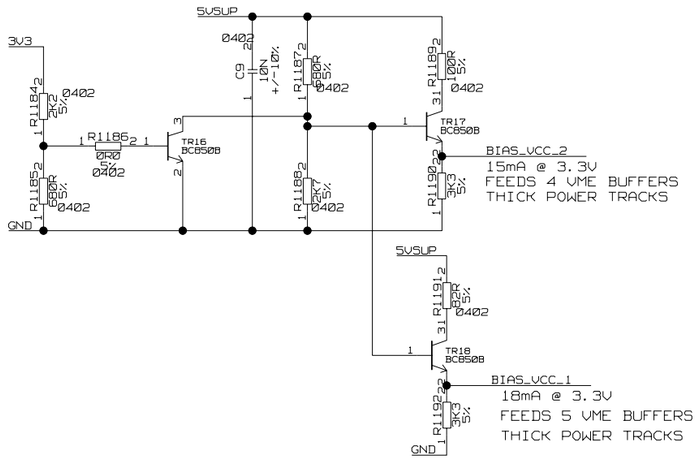
CMS TRACKER FED
TTC RECEIVER AND PIN DIODE CONNECTOR

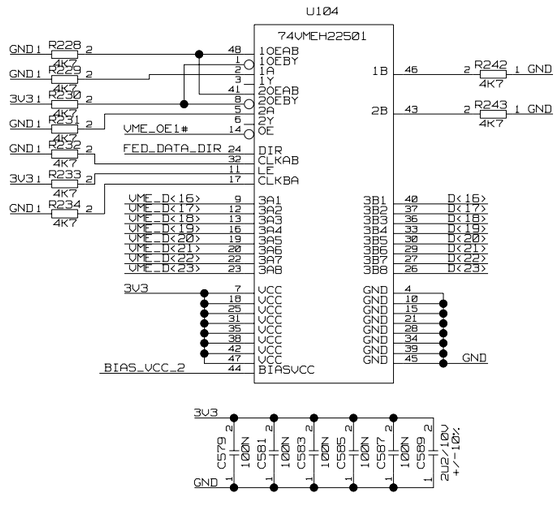
A 2-TE-0070-020-05-B

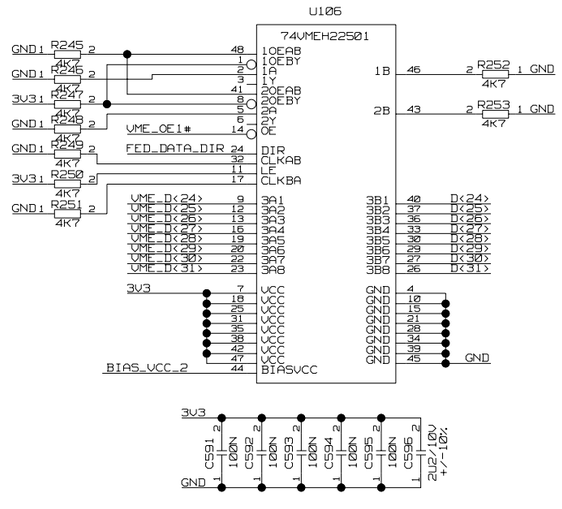
TOTAL NO. OF SHEETS 95

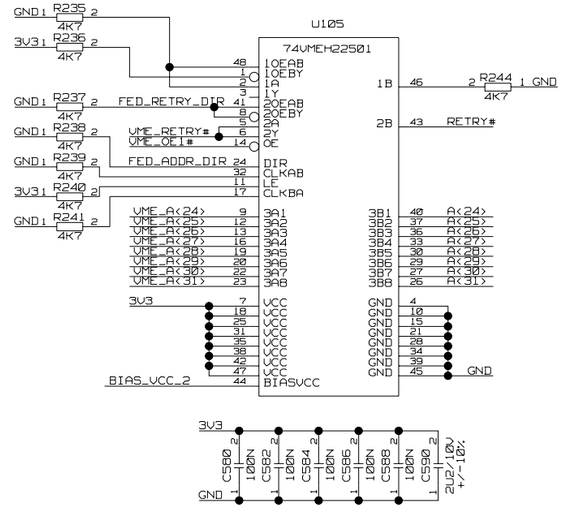
A 2 -TE-0070-020-05-B

A	2-TE-0070-020-06-B	THIS DRAWING CONFORMS TO B.S. 3939							









B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED

J2 VME INTERFACE AND PRECHARGE CIRCUIT

A2-TE-0070-020-06-B

TOTAL NO. OF SHEETS 95

A2-TE-0070-020-06-B

A | 2-TE-0070-020-07-B | THIS DRAWING CONFORMS TO B.S. 3939

B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	S.TAGHAVIRAD	S.TAGHAVIRAD	S.TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

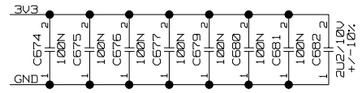
TITLE PC3205M CIRCUIT

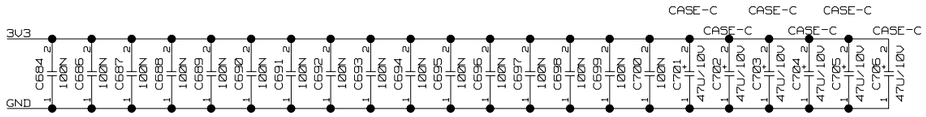
CMS TRACKER FED
VME FPGA

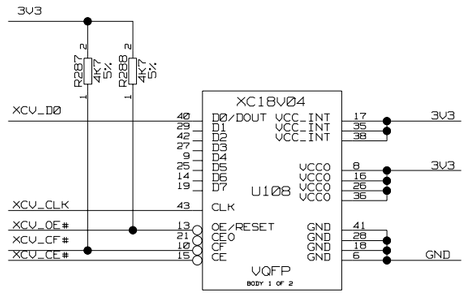
A | 2-TE-0070-020-07-B

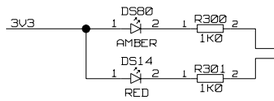
TOTAL NO. OF SHEETS 95

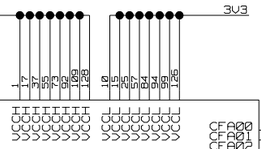
A	2-TE-0070-020-08-B	THIS DRAWING CONFORMS TO B.S. 3939

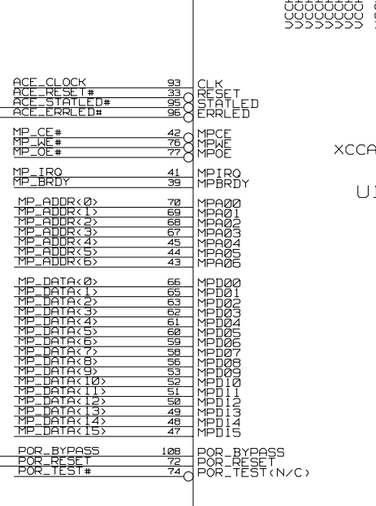


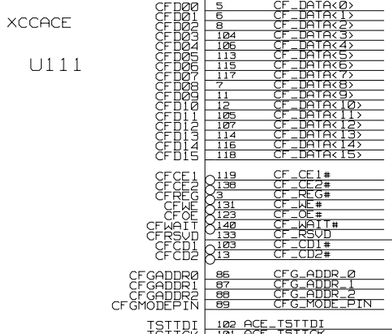




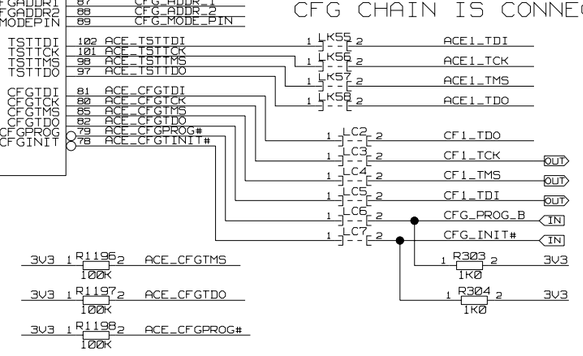


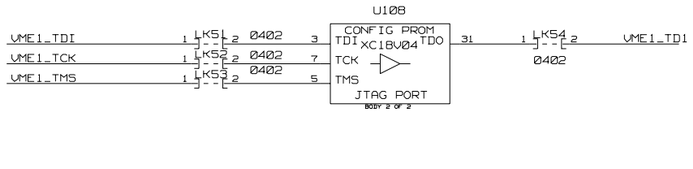


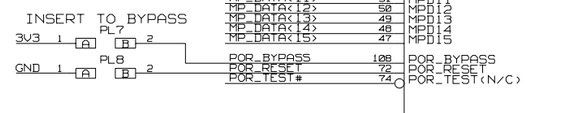


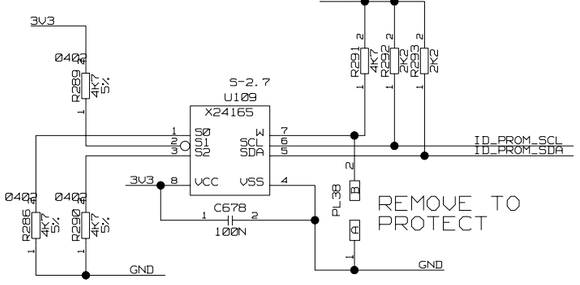


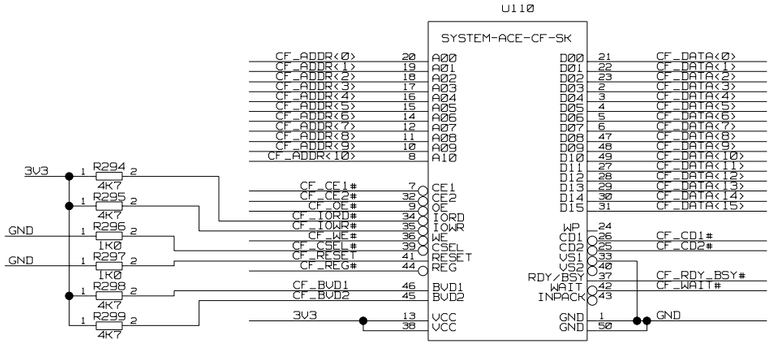
CFG CHAIN IS CONNECTED TO TST CHAIN.











B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	S.TAGHAVIRAD	S.TAGHAVIRAD	S.TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS

RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

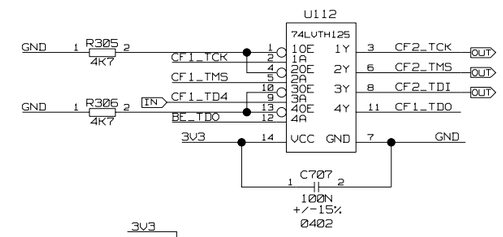
CMS TRACKER FED

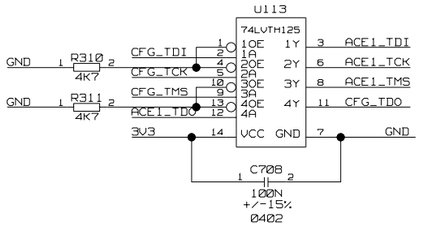
SYSTEM ACE AND CONFIGURATION DEVICE

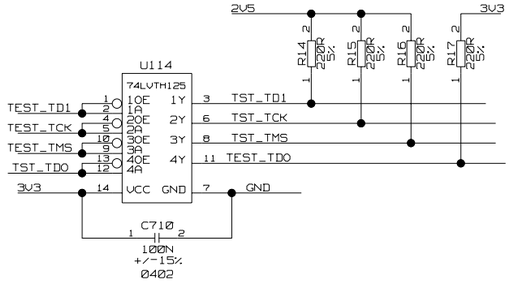
A 2-TE-0070-020-08-B

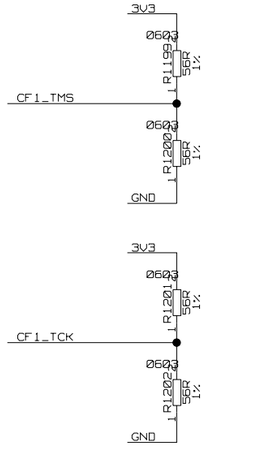
TOTAL NO. OF SHEETS 95

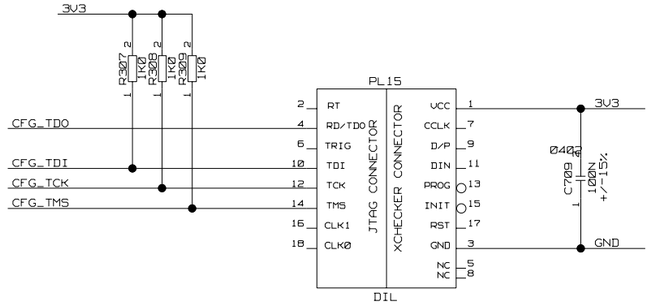
A 2-TE-0070-020-08-B

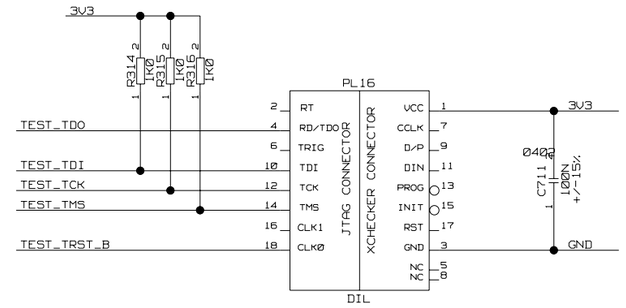


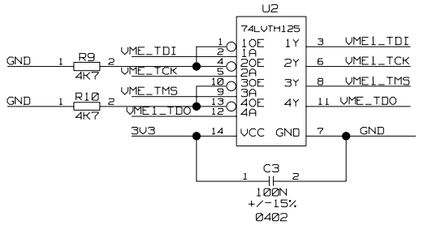


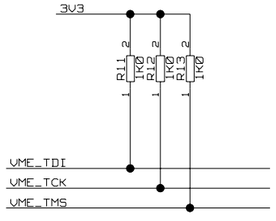












ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

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COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

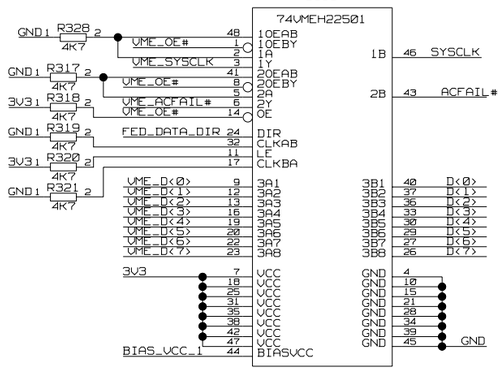
CMS TRACKER FED
JTAG CONNECTORS AND BUFFERS

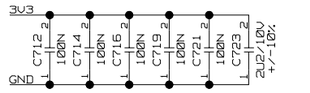
A 2-TE-0070-020-09-B

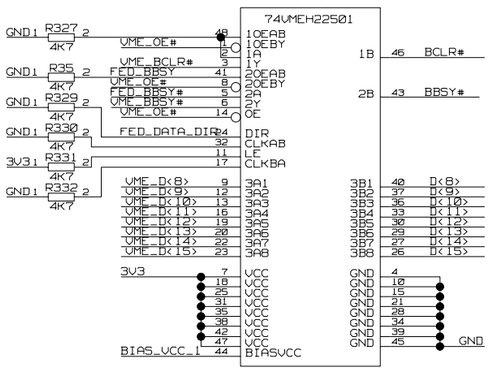
TOTAL NO. OF SHEETS 95

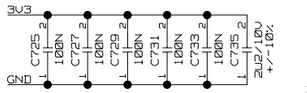
A 2-TE-0070-020-09-B

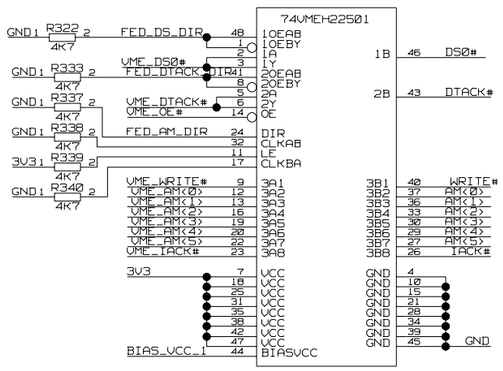
A	2-TE-0070-020-10-B	THIS DRAWING CONFORMS TO B.S. 3939

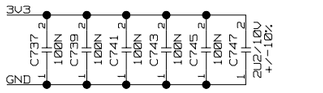


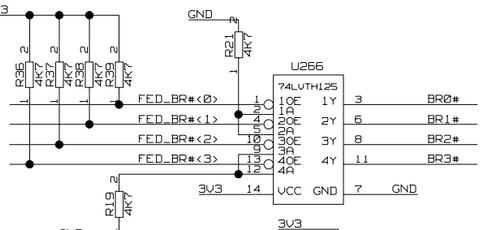


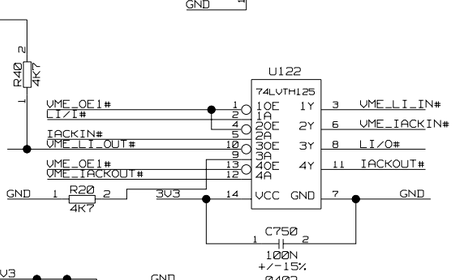


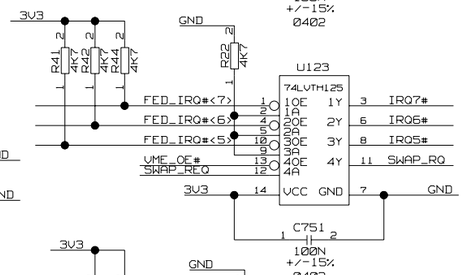


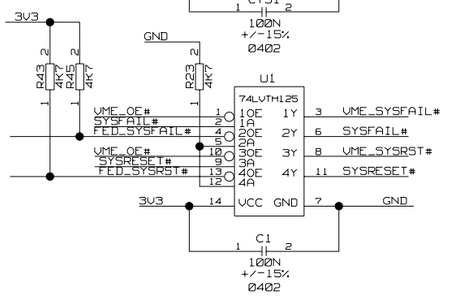


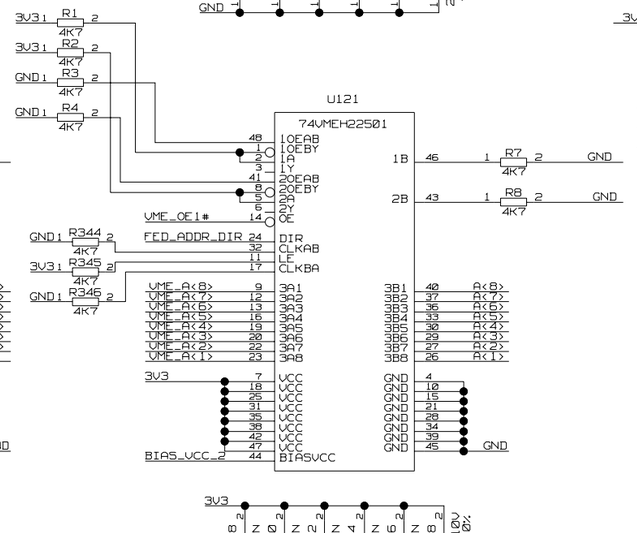


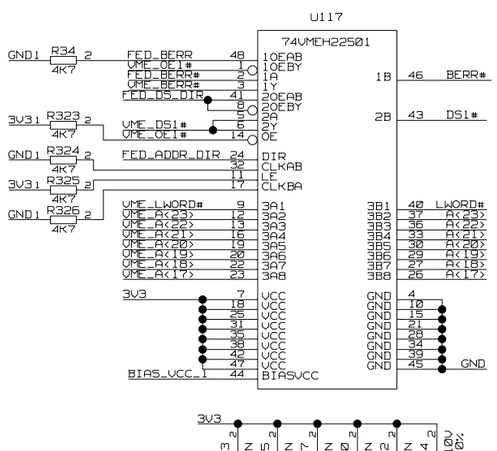


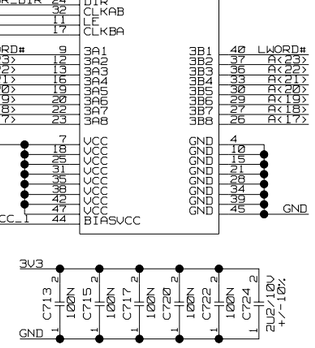


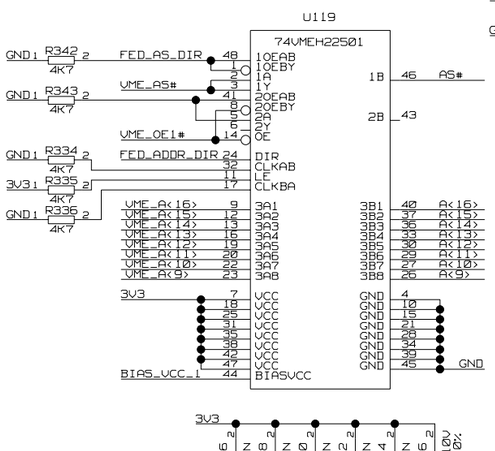


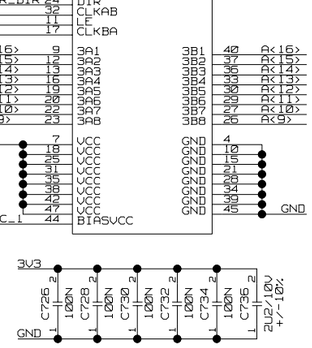


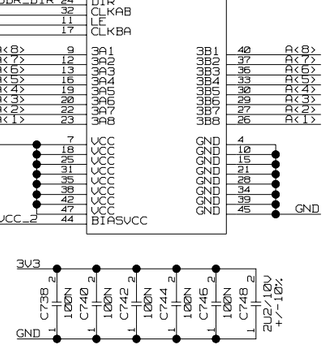


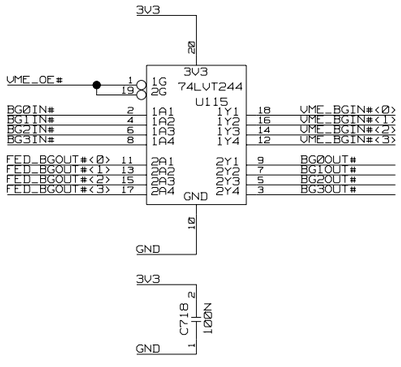












ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED
J1 VME INTERFACE

A 2-TE-0070-020-10-B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020-10-B

A	2-TE-0070-020-11-B	THIS DRAWING CONFORMS TO B.S. 3939	

J0

SK-HARBUSHM-SHIELDED-95

SK9

TTS_J0_READY
TTS_J0_READY_B
TTS_J0_BUSY
TTS_J0_BUSY_B
TTS_J0_WARN_OVRFLW
TTS_J0_WARN_OVRFLW_B
TTS_J0_OUT_OF_SYNC
TTS_J0_OUT_OF_SYNC_B
BE_J0_SPARE<0>
BE_J0_SPARE<1>
BE_J0_SPARE<2>
BE_J0_SPARE<3>
TEST_TRIG
TEST_TRIG_B
TEST_CLK
TEST_CLK_B
VME_J0_SPARE<0>
VME_J0_SPARE<1>
3V3
VME_TMS
VME_TCK
VME_TDI
GND
VME_TMS
VME_TCK
VME_TDO

3V3
C14 100N 0402 +/-5%
GND
PLACE CLOSE TO J0

J1

PL-HARBUS64-160

PL17

D<0>
BBSY#
GND
D<1>
BCLR#
D<2>
ACFAIL#
D<3>
BG0IN#
D<4>
BG0OUT#
D<5>
BG1IN#
D<6>
BG1OUT#
D<7>
BG2IN#
BG2OUT#
SYSCLK
BG3IN#
RESP#
BG3OUT#
DS1#
BR0#
DS0#
BR1#
WRITE#
BR2#
BR3#
DTACK#
AM<0>
AM<1>
AS#
AM<2>
AM<3>
IACK#
IACKIN#
SERA
IACKOUT#
SERB
AM<4>
A<7>
IRQ7#
A<6>
IRQ6#
A<5>
IRQ5#
A<4>
IRQ4#
A<3>
IRQ3#
A<2>
IRQ2#
A<1>
IRQ1#
-12VIN
+5VIN
+5VIN

D<8>
+5VIN
D<9>
GND
D<10>
+V1
D<11>
+V2
D<12>
D<13>
-V1
D<14>
-V2
D<15>
GAP#
SYSFAIL#
GA0#
BERR#
GA1#
SYSRESET#
3V3IN
LWORD#
GA2#
AM<5>
A<23>
GA3#
A<22>
A<21>
GA4#
A<20>
A<19>
A<18>
A<17>
A<16>
A<15>
A<14>
A<13>
A<12>
A<11>
LI/I#
A<10>
A<9>
LI/O#
A<8>
+12VIN
+5VIN
+5VIN

J2

PL-HARBUS64-160

PL18

SLINK_UD<4>
+5VIN
GND
SLINK_UD<5>
SLINK_URESET#
SLINK_UD<2>
RETRY#
SLINK_UD<3>
A<24>
SLINK_UTEST#
SLINK_UD<14>
A<25>
SLINK_UD<15>
A<26>
SLINK_UCNTL#
SLINK_UD<16>
A<27>
SLINK_UD<17>
A<28>
SLINK_UDW1
SLINK_UD<10>
A<29>
SLINK_UD<11>
A<30>
SLINK_UDW0
SLINK_UD<24>
A<31>
SLINK_UD<25>
SLINK_UWEN#
SLINK_UD<18>
SLINK_UD<19>
D<16>
SLINK_UD<36>
D<17>
SLINK_UD<37>
D<18>
SLINK_USF<3>
SLINK_UD<32>
D<19>
SLINK_UD<33>
D<20>
SLINK_USF<2>
SLINK_UD<34>
D<21>
SLINK_UD<35>
D<22>
SLINK_USF<1>
SLINK_UD<46>
D<23>
SLINK_UD<47>
SLINK_USF<0>
SLINK_UD<45>
D<24>
SLINK_UD<44>
D<25>
SLINK_LFF#
SLINK_UD<61>
D<26>
SLINK_UD<60>
D<27>
SLINK_LRL<3>
SLINK_UD<49>
D<28>
SLINK_UD<48>
D<29>
SLINK_LRL<2>
SLINK_UD<50>
D<30>
SLINK_UD<51>
D<31>
SLINK_LRL<1>
SLINK_UD<55>
SLINK_UD<54>

SLINK_UD<22>
SLINK_UD<23>
SLINK_UD<12>
SLINK_LRL<0>
SLINK_UD<13>
SLINK_LDOWN#
SLINK_UD<0>
SLINK_LSF<3>
SLINK_UD<1>
SLINK_LSF<2>
SLINK_UD<6>
SLINK_LSF<1>
SLINK_UD<7>
SLINK_LSF<0>
SLINK_UD<8>
SLINK_UCLK
SLINK_UD<9>
SLINK_UCLK_B
SLINK_UD<20>
SLINK_UD<21>
SLINK_UD<26>
SLINK_UD<27>
SLINK_UD<28>
SLINK_UD<29>
SLINK_UD<30>
SLINK_UD<31>
SLINK_UD<41>
SLINK_UD<40>
SLINK_UD<39>
SLINK_UD<38>
SLINK_UD<53>
TTS_J2_READY
SLINK_UD<52>
TTS_J2_BUSY
SLINK_UD<43>
TTS_J2_WARN_OVRFLW
SLINK_UD<42>
TTS_J2_OUT_OF_SYNC
SLINK_UD<59>
BE_J2_SPARE<0>
SLINK_UD<58>
BE_J2_SPARE<1>
SLINK_UD<63>
SLINK_UD<62>
SLINK_UD<57>
GND
SLINK_UD<56>
+5VIN

R24 2K7 0402 5%
GND

0402 R1203 100R 5%
TEST_CLK
TEST_CLK_B

0402 R1204 100R 5%
DO NOT FIT.
BE_J0_SPARE<0>
BE_J0_SPARE<1>

0402 R1205 100R 5%
DO NOT FIT.
BE_J0_SPARE<2>
BE_J0_SPARE<3>

0402 R1206 100R 5%
TEST_TRIG
TEST_TRIG_B

DO NOT FIT.
0402 R1211 100R 5%
VME_J0_SPARE<0>
VME_J0_SPARE<1>

0402 R1212 100R 5%
SLINK_UD<10>
SLINK_UD<11>

0402 R1213 100R 5%
SLINK_UD<12>
SLINK_UD<13>

0402 R1214 100R 5%
SLINK_UD<45>
SLINK_UD<44>

0402 R1215 100R 5%
SLINK_UD<43>
SLINK_UD<42>

THESE RESISTORS ARE
DO NOT FIT.

PLACE RESISTORS AT DESTINATION

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

USED ON CMS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED
CONNECTORS

A2-TE-0070-020-11-B

TOTAL NO. OF SHEETS 95

A2-TE-0070-020-11-B

A | 2-TE-0070-020-12-B | THIS DRAWING CONFORMS TO B.S. 3939

+12VIN
0603
C339
100N
+/-10%
GND

U128
TP5351Ø
ACFAIL# 1 PGI PGO 8 POWER_IN_OK
TP104 BLACK FP0# 3 FP0* VDD 7 +12VIN
PSON# 4 PSON* VSS 6 R361 2 +5VIN
GND 2 GND VS33 5 R362 2 3V3IN
470R 2010 1%
470R 2010 1%

0402
+12VIN R1229 2
4K7 5%
0402 R1230 2 GND
3K3 5%

U133
HEF4073B
I1 I2 I3 VDD 14 5VSUP
O1 6 5V_3V3_EN
PGOOD-5VA PGOOD+12V I4 I5 I6 O2 9 PGOOD
5V_3V3_EN PGOOD+5V PGOOD+1V5 I7 I8 I9 O3 10 12V_EN
VSS 7 GND

U131
HEF4073B
I1 I2 I3 VDD 14 5VSUP
O1 6 TSHDOWN#
PGOOD+5V PGOOD+2V5 PGOOD+3V3 I4 I5 I6 O2 9
I7 I8 I9 O3 10
VSS 7 GND
R1235 2
4K7 5%

1V5
R25 2 1K0 1% 0603
R26 2 10K 5% 0402
C16 2 100N +/-10% 0603
GND

U6
MAX708
MR RESET 2
RESET 1
PFI PFO 7 PGOOD+1V5
VCC 4 GND 5
NC 8
5VSUP
SW1 SK-12D40
C15 2 100N +/-10% 0603
GND

PSON#
0402 LK59 2

0402
GND R46 2 4K7 5%

U129
HEF40240B
VDD 20
EOA EOB 19
+5VIN 3V3IN PGOOD+1V5 TSHDOWN# IA1 IA2 IA3 IA4 2 4 6 8
+12VIN PGOOD-5VA PGOOD+2V5 PGOOD IB1 IB2 IB3 IB4 11 13 15 17
OA1 OA2 OA3 OA4 18 16 14 12
1V5GOOD 14
OB1 OB2 OB3 OB4 9 7 5 3
VSS 10
GND

DS81 R1221 2 2K2 RED
DS82 R1222 2 2K2 RED
DS83 R1223 2 2K2 RED
DS84 R1224 2 2K2 RED
DS85 R1225 2 2K2 RED
DS86 R1226 2 2K2 RED
DS87 R1227 2 2K2 RED
DS88 R1228 2 2K2 RED
PGOOD_LED GND

5VSUP
R1231 2 4K7 5%
R1232 2 4K7 5%
R1233 2 4K7 5%

0402 LK71 2
0402 LK72 2
0402 LK73 2

IO +5V
IO 3V3
IO 1V5
IN 5VA_NEG
IO GND

3V3
RN31 1K0 5%
U124
TCMT4100
IN T_CRIT_1# 1 AN1 CA1 COL1 EM1 16
IN T_CRIT_2# 2 AN2 CA2 COL2 EM2 15
IN T_CRIT_3# 3 AN3 CA3 COL3 EM3 14
IN T_CRIT_4# 4 AN4 CA4 COL4 EM4 13
5VSUP

3V3
RN32 1K0 5%
U125
TCMT4100
IN T_CRIT_5# 1 AN1 CA1 COL1 EM1 16
IN T_CRIT_6# 2 AN2 CA2 COL2 EM2 15
IN T_CRIT_7# 3 AN3 CA3 COL3 EM3 14
IN T_CRIT_8# 4 AN4 CA4 COL4 EM4 13
5VSUP

3V3
RN33 1K0 5%
U126
TCMT4100
VME_T_CRIT# 1 AN1 CA1 COL1 EM1 16
BE_T_CRIT# 2 AN2 CA2 COL2 EM2 15
PG+2V5# 3 AN3 CA3 COL3 EM3 14
PGOOD_LED R1215 2 3K3 7 AN4 CA4 COL4 EM4 13
GND 8 10 9
PGOOD+2V5
MAX823_MR#
GND
0402 R157 2 10K 5% GND

FIT 1.5A FUSE
+5VIN FS1 SMF 5A 2
5VSUP
C753 2 10N
C754 2 10N
C755 2 10N
C756 2 10N
C758 2 10N
C759 2 10N
C760 2 10N
C761 2 10N
C762 2 10N
C763 2 10N
C764 2 2U2/10V +/-10%
GND

GND
5VSUP
R1217 2 4K7 5%
RN34 10K 5%
U2670Ø
VDD HEF4043B
S0 R0 4 3
S1 R1 6 7
S2 R2 12 11
S3 R3 14 15
EO 5
VSS 8
O1 9
O2 10
O3 1
NC 13
5VSUP
R1218 2 4K7 5%
GND
LK63 2
LK64 2
LK65 2
LK66 2
LK60 2

GND
5VSUP
RN35 10K 5%
U2680Ø
VDD HEF4043B
S0 R0 4 3
S1 R1 6 7
S2 R2 12 11
S3 R3 14 15
EO 5
VSS 8
O1 9
O2 10
O3 1
NC 13
5VSUP
R1219 2 4K7 5%
GND
LK67 2
LK68 2
LK69 2
LK70 2

GND
5VSUP
RN36 10K 5%
U2690Ø
VDD HEF4043B
S0 R0 4 3
S1 R1 6 7
S2 R2 12 11
S3 R3 14 15
EO 5
VSS 8
O1 9
O2 10
O3 1
NC 13
5VSUP
R1220 2 4K7 5%
GND
0402 LK61 2
0402 LK62 2

PL19 1A SWAP_GRANTED
2A GRANT_SWAP
3A SWAP_REQ 1 A
PL20 2 B
0402 R359 2 4K7 5% GND
5VSUP

U130
HEF4002B
VDD 14 5VSUP
I1 I2 I3 I4 2 3 4 5
O1 1
O2 13
I5 I6 I7 I8 9 10 11 12
NC1 6
NC2 8
VSS 7 GND

U132
HEF4002B
VDD 14 5VSUP
I1 I2 I3 I4 2 3 4 5
O1 1
O2 13 PWR_UP_FAIL
5V_3V3_EN I2V_EN PGOOD-5VA PGOOD+2V5 I5 I6 I7 I8 9 10 11 12
NC1 6
NC2 8
VSS 7 GND
SWAP#

B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	J. SALISBURY	J. SALISBURY	J. SALISBURY	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

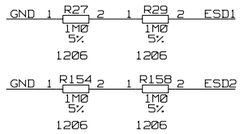
TITLE
PC3205M CIRCUIT
CMS TRACKER FED
OPTO ISOLATION AND FAULT SIGNAL LATCHING

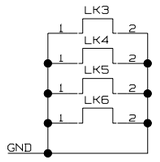
A 2-TE-0070-020-12-B

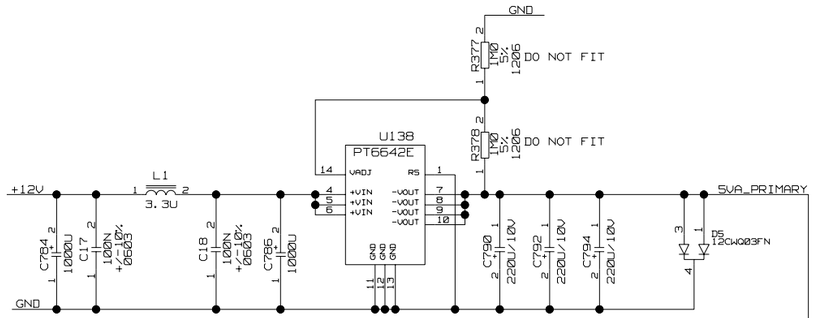
TOTAL NO. OF SHEETS 95

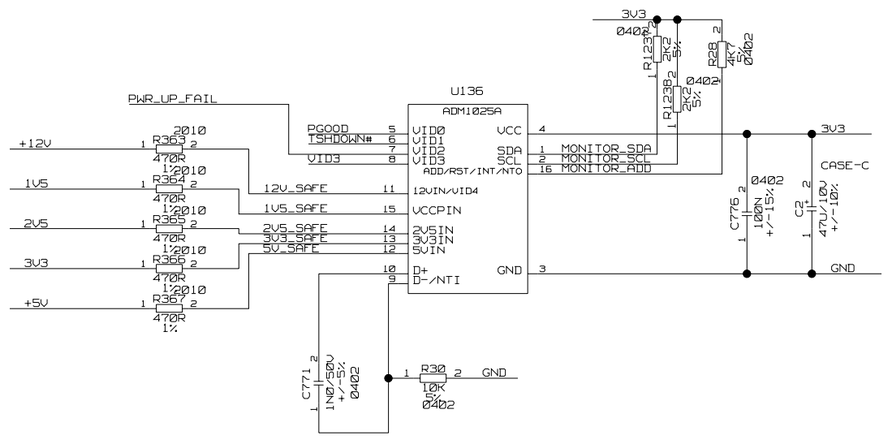
A 2-TE-0070-020-12-B

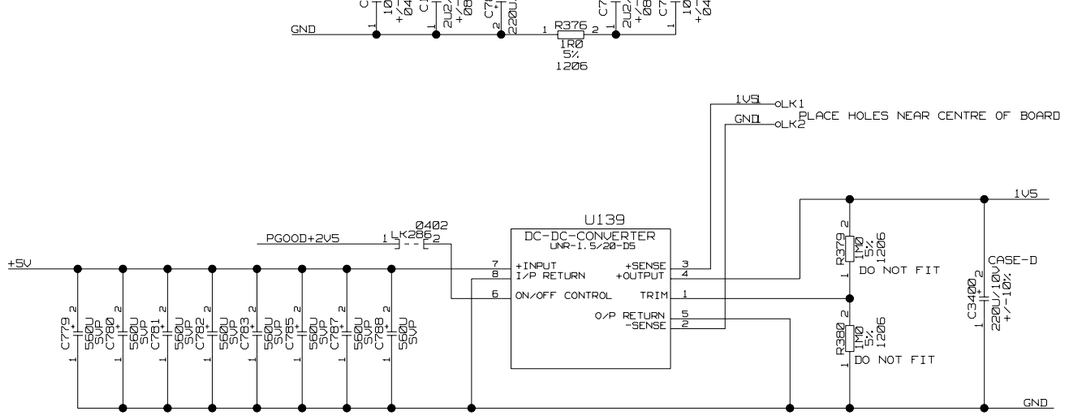
A	2-TE-0070-020-13-B	THIS DRAWING CONFORMS TO B.S. 3939							

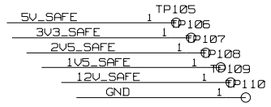


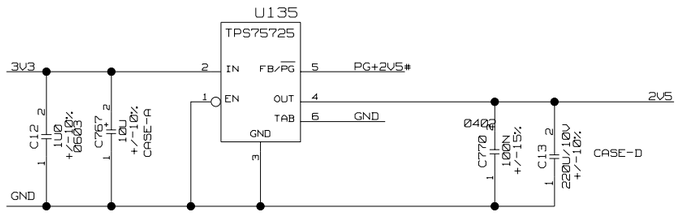




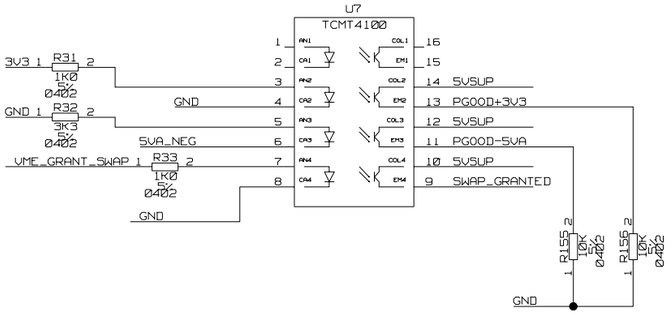








TPS75725 IS CONDITIONALLY STABLE
CONSULT DATA SHEET BEFORE CHANGING CAPACITORS



B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	J.SALISBURY	J.SALISBURY	J.SALISBURY	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

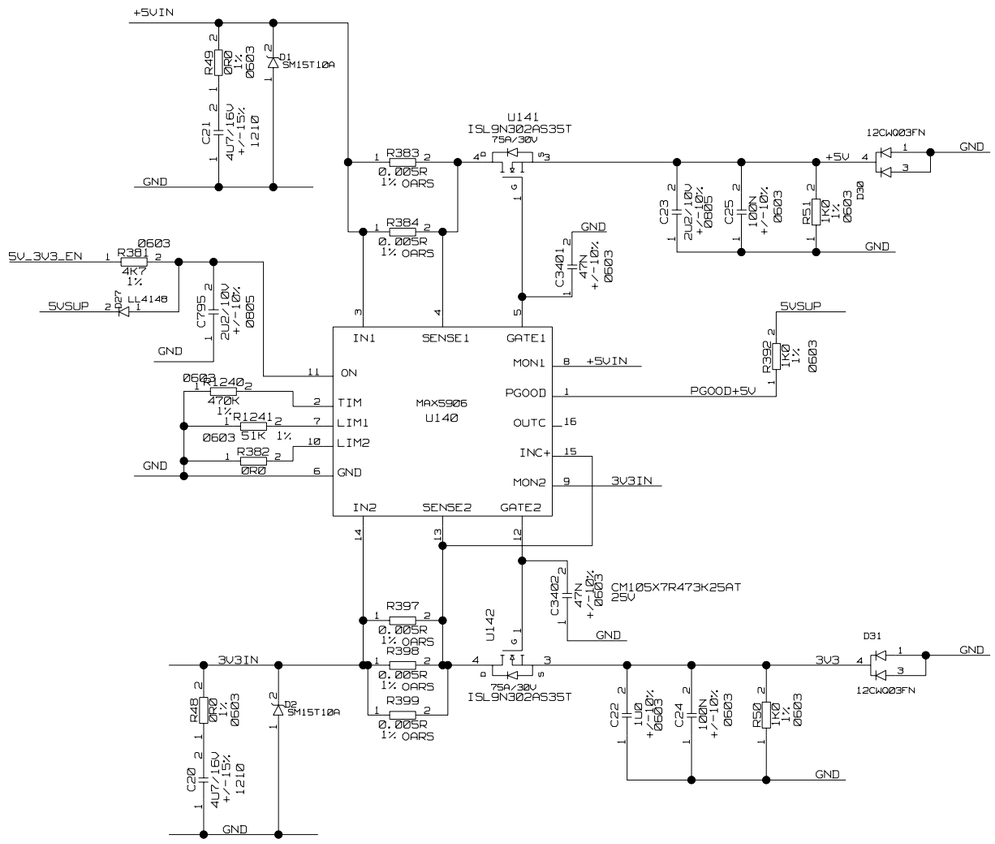
PC3205M CIRCUIT

CMS TRACKER FED
DC-DC CONVERTORS AND MONITORING

A 2-TE-0070-020-13-B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020-13-B



B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	J. SALISBURY	J. SALISBURY	J. SALISBURY	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

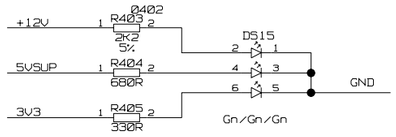
CMS TRACKER FED

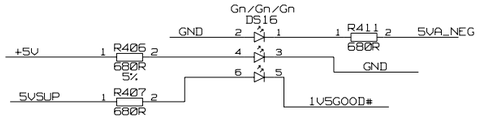
ELECTRONIC POWER SUPPLY PROTECTION

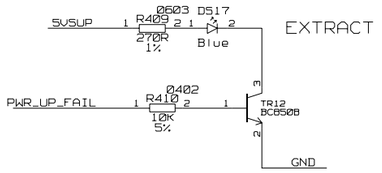
A2-TE-0070-020-14-B

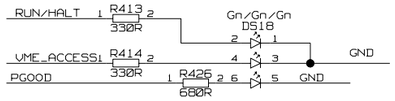
TOTAL NO. OF SHEETS 95

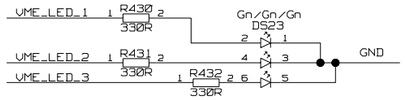
A2-TE-0070-020-14-B

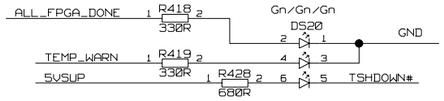


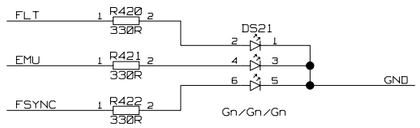


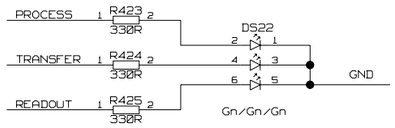


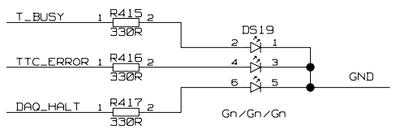












B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	J. SALISBURY	J. SALISBURY	J. SALISBURY	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

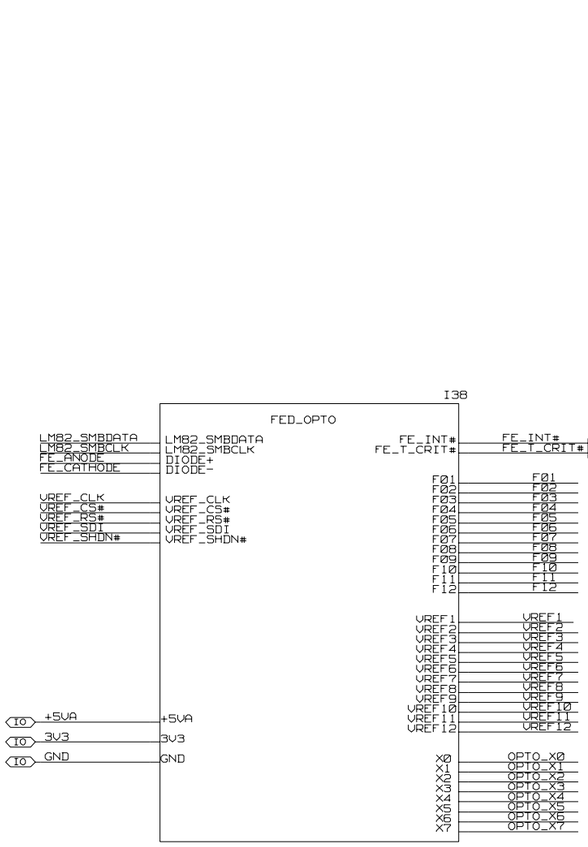
CMS TRACKER FED
FRONT PANEL DISPLAY

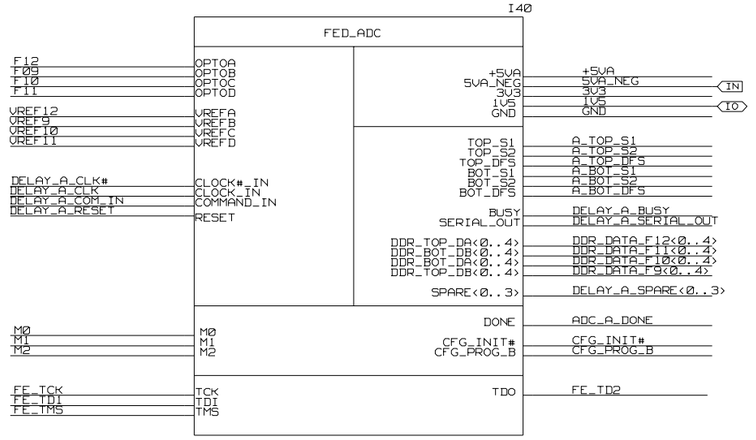
A 2-TE-0070-020-15-B

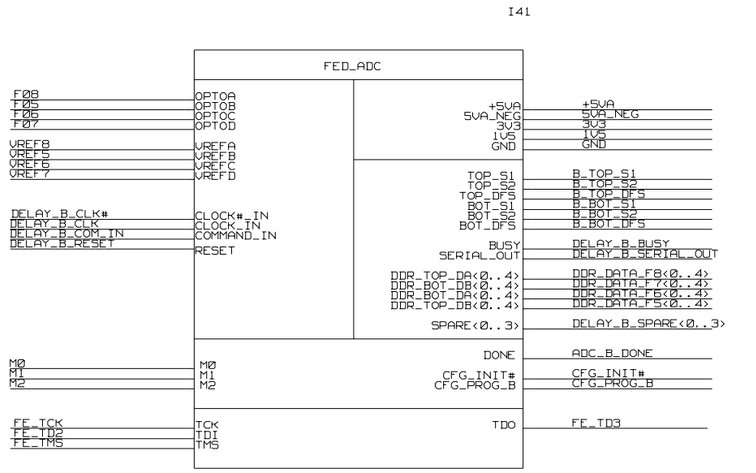
TOTAL NO. OF SHEETS 95

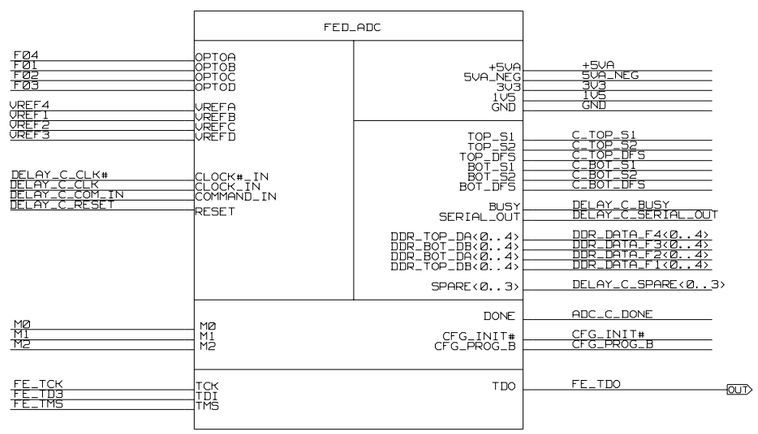
A 2 -TE-0070-020-15-B

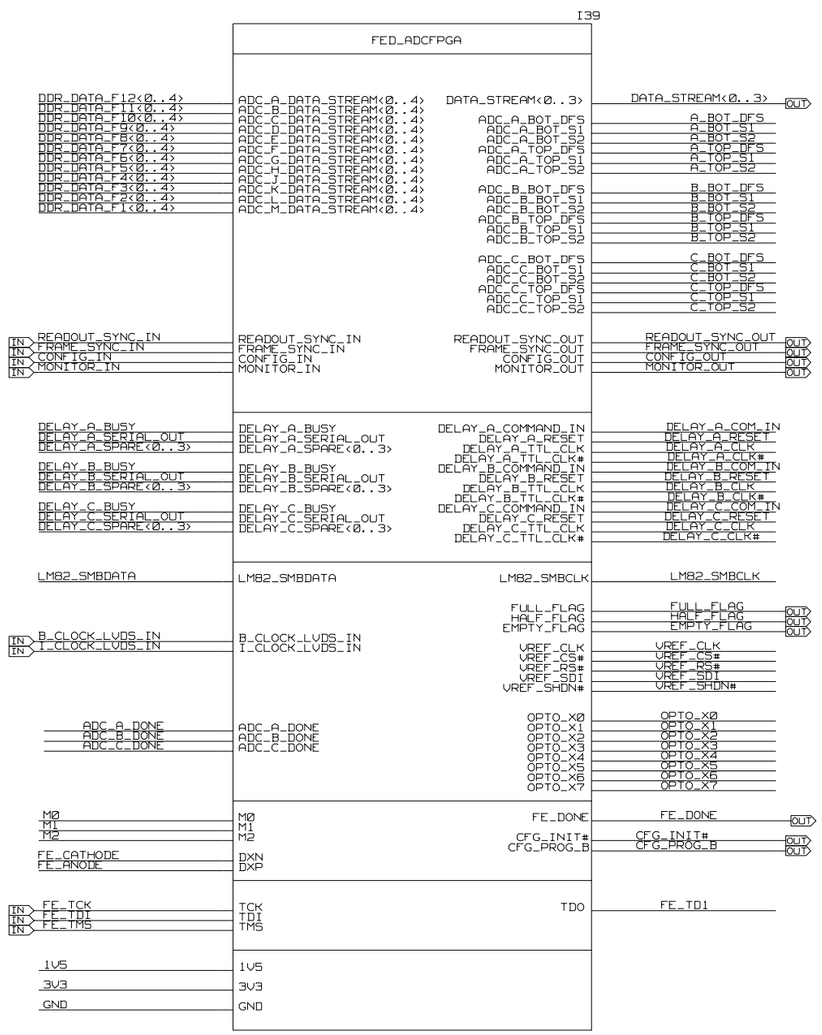
A	2-TE-0070-020<16>B	THIS DRAWING CONFORMS TO B.S. 3939











ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS

RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

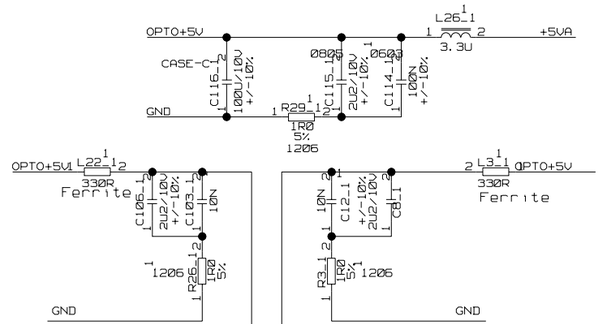
CMS TRACKER FED

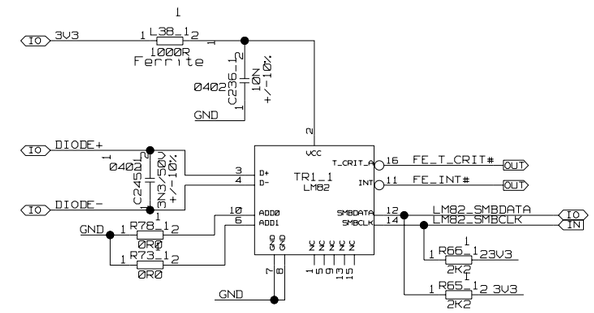
CHANNEL

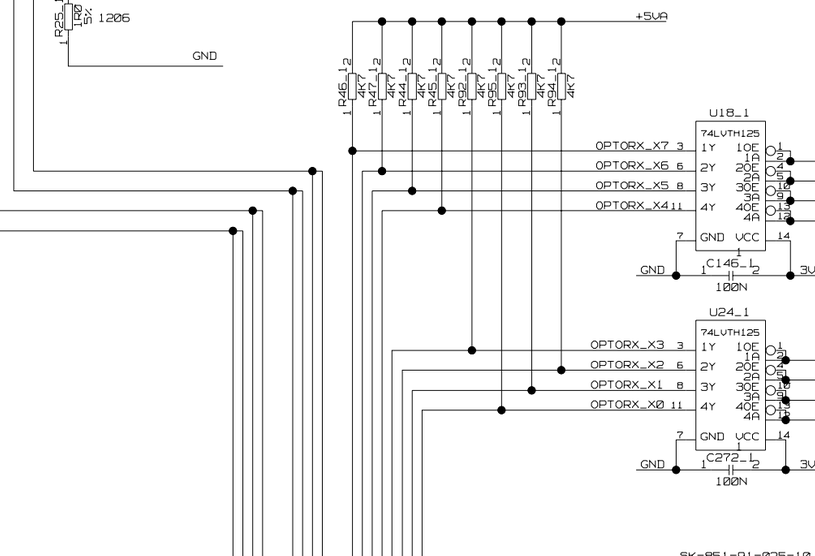
A | 2-TE-0070-020<16>B

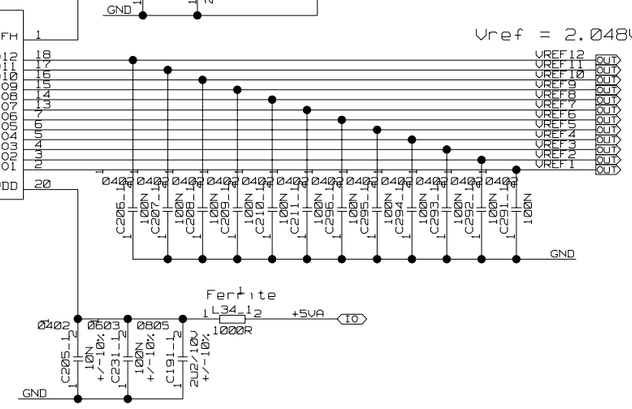
TOTAL NO. OF SHEETS 95

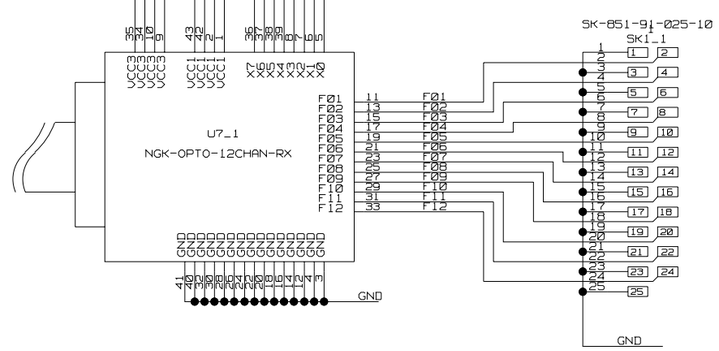
A | 2-TE-0070-020<16>B











B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	J.SALISBURY	J.SALISBURY	J.SALISBURY	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

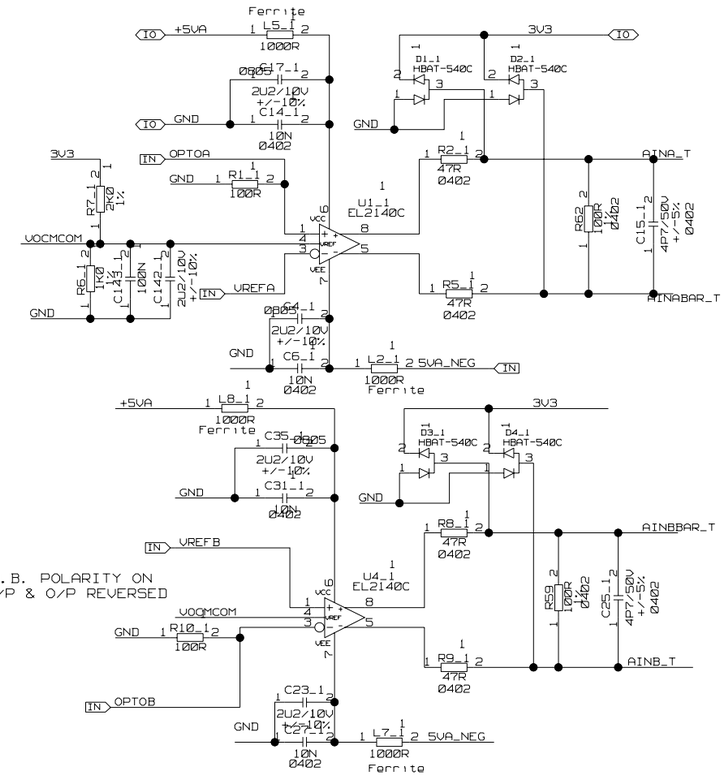
CMS TRACKER FED
OPTO RXR AND VREF GENERATOR

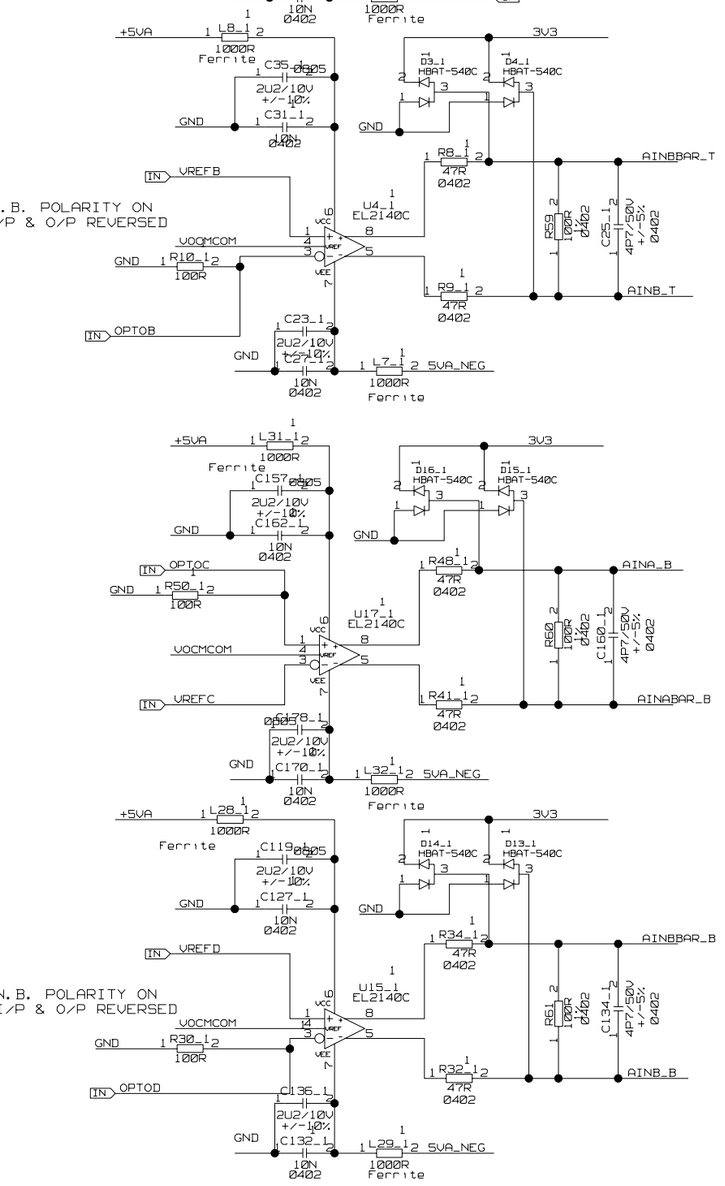
A 2-TE-0070-020<17>B

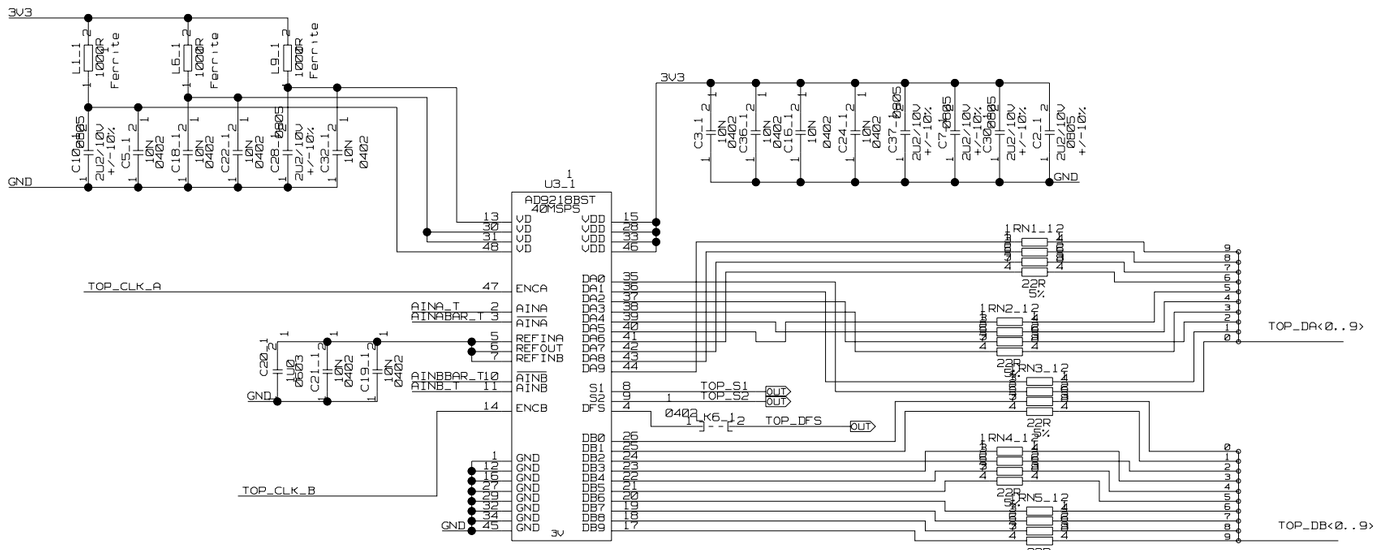
TOTAL NO. OF SHEETS 95

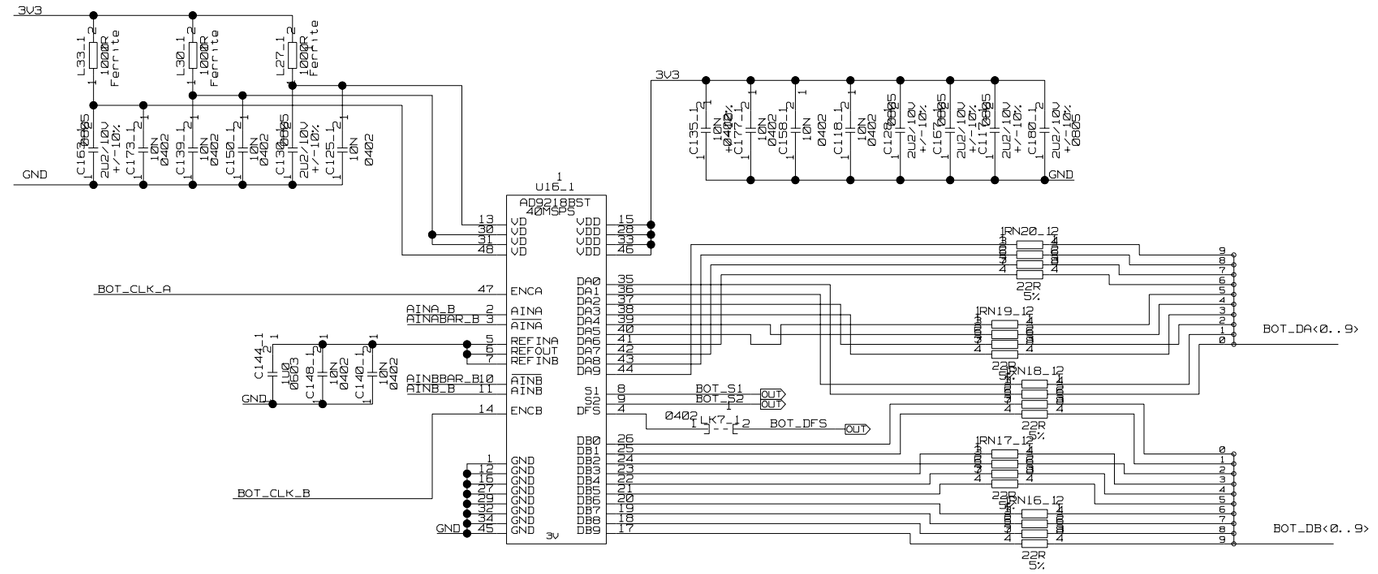
A 2-TE-0070-020<17>B

A | 2-TE-0070-020<18>B | THIS DRAWING CONFORMS TO B.S. 3939









ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	J.SALISBURY	J.SALISBURY	J.SALISBURY	

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

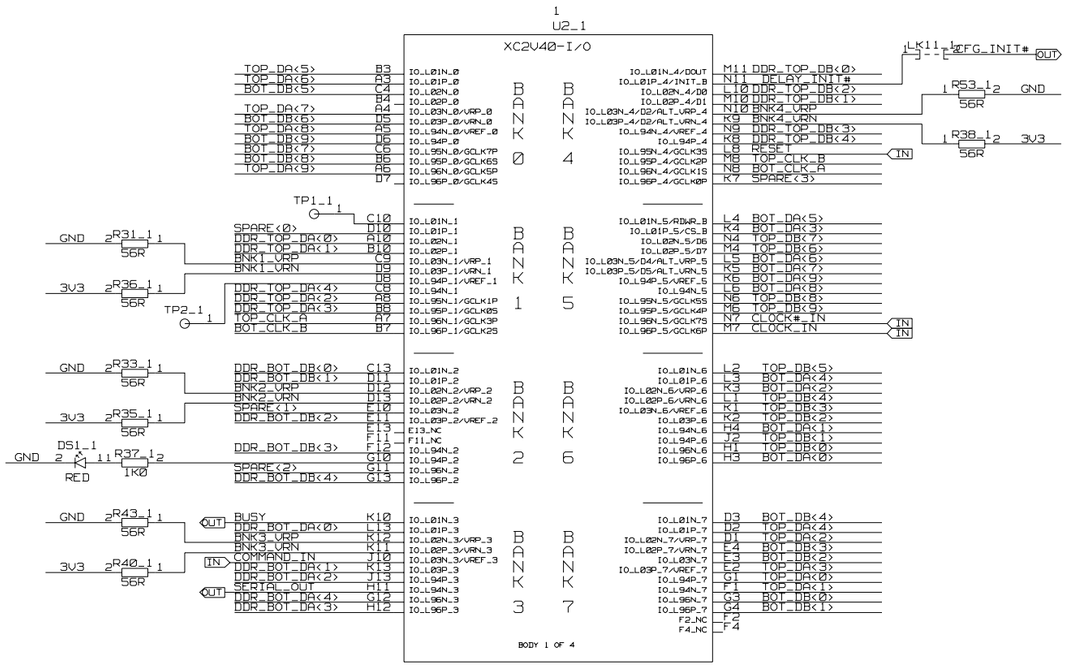
CMS TRACKER FED

DIFFERENTIAL OP AMPS AND 10 BIT ADCS

A2-TE-0070-020<18>B

TOTAL NO. OF SHEETS 95

A	2-TE-0070-020<19>B	THIS DRAWING CONFORMS TO B.S. 3939



B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED DELAY FPGA

A 2-TE-0070-020<19>B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020<19>B

A | 2-TE-0070-020<18>B | THIS DRAWING CONFORMS TO B.S. 3939

N.B. POLARITY ON I/P & O/P REVERSED

N.B. POLARITY ON I/P & O/P REVERSED

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	J.SALISBURY	J.SALISBURY	J.SALISBURY	

USED ON CMS

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

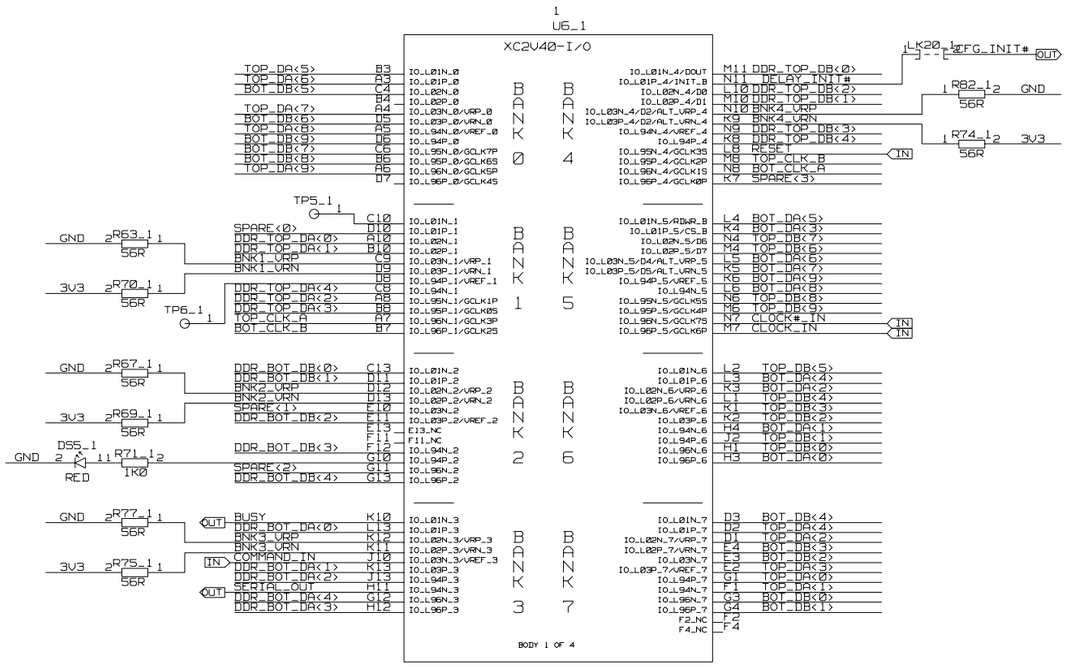
PC3205M CIRCUIT

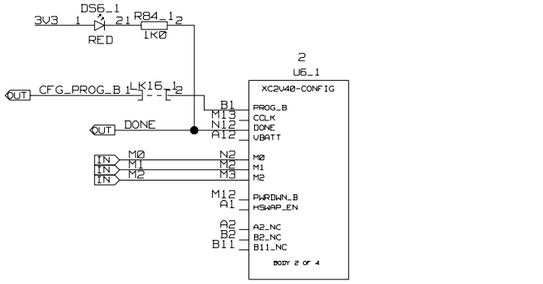
CMS TRACKER FED

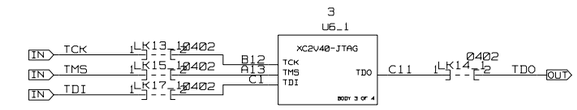
DIFFERENTIAL OP AMPS AND 10 BIT ADCS

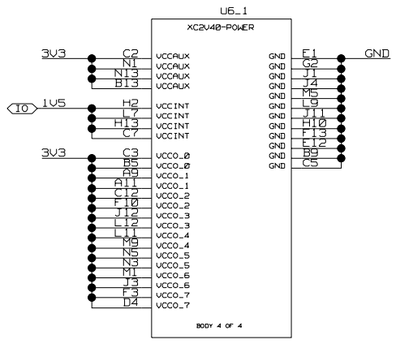
A2-TE-0070-020<18>B

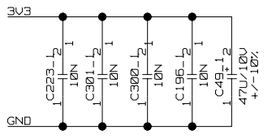
TOTAL NO. OF SHEETS 95

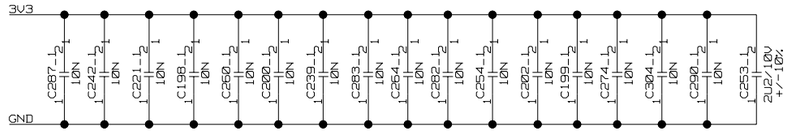


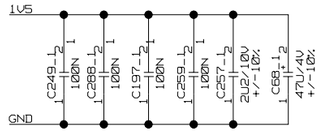












B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON CMS

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CCLRC
COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

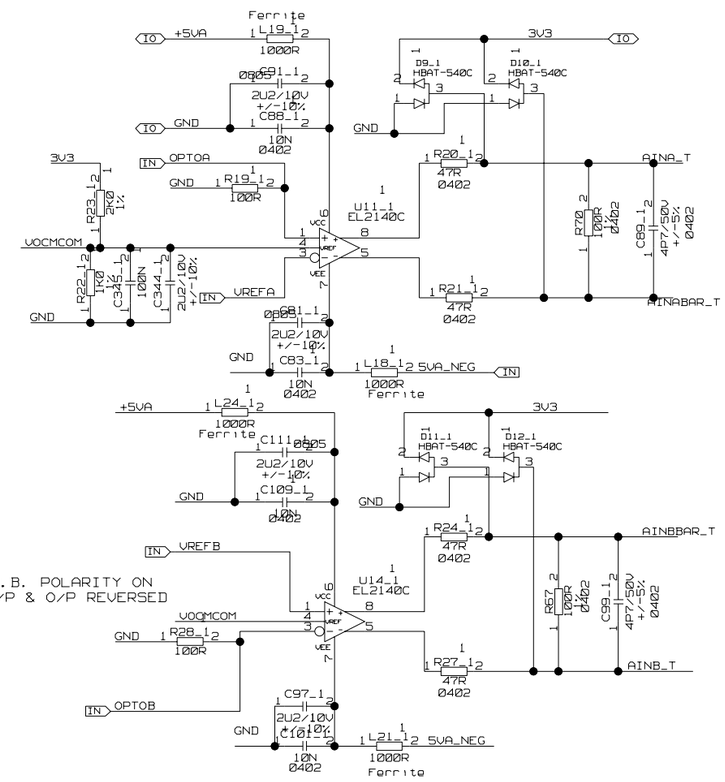
CMS TRACKER FED
DELAY FPGA

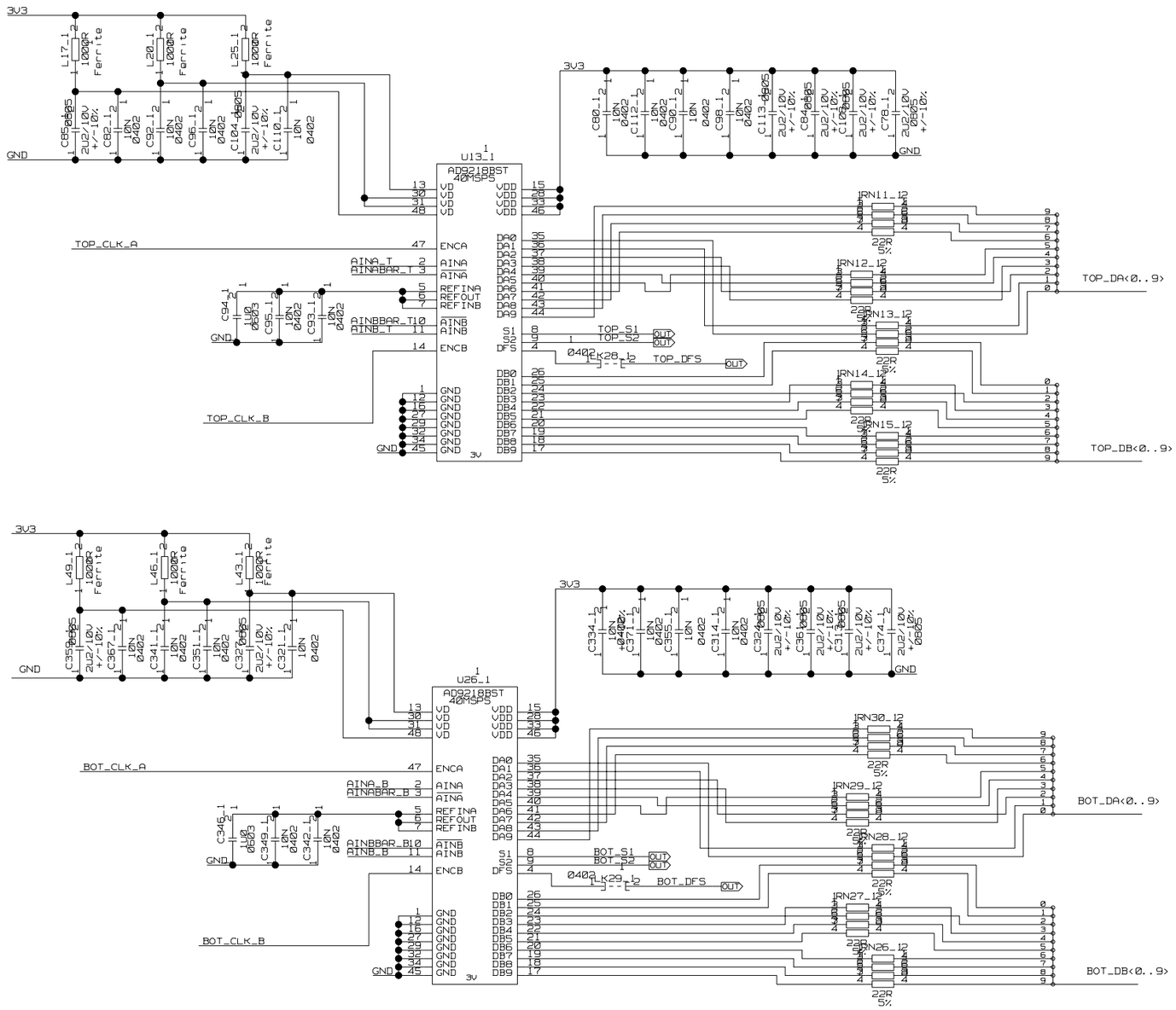
A 2-TE-0070-020<19>B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020<19>B

A | 2-TE-0070-020<18>B | THIS DRAWING CONFORMS TO B.S. 3939





ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	J.SALISBURY	J.SALISBURY	J.SALISBURY	

USED ON CMS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3205M CIRCUIT

CMS TRACKER FED

DIFFERENTIAL OP AMPS AND 10 BIT ADCS

A2-TE-0070-020<18>B

TOTAL NO. OF SHEETS 95

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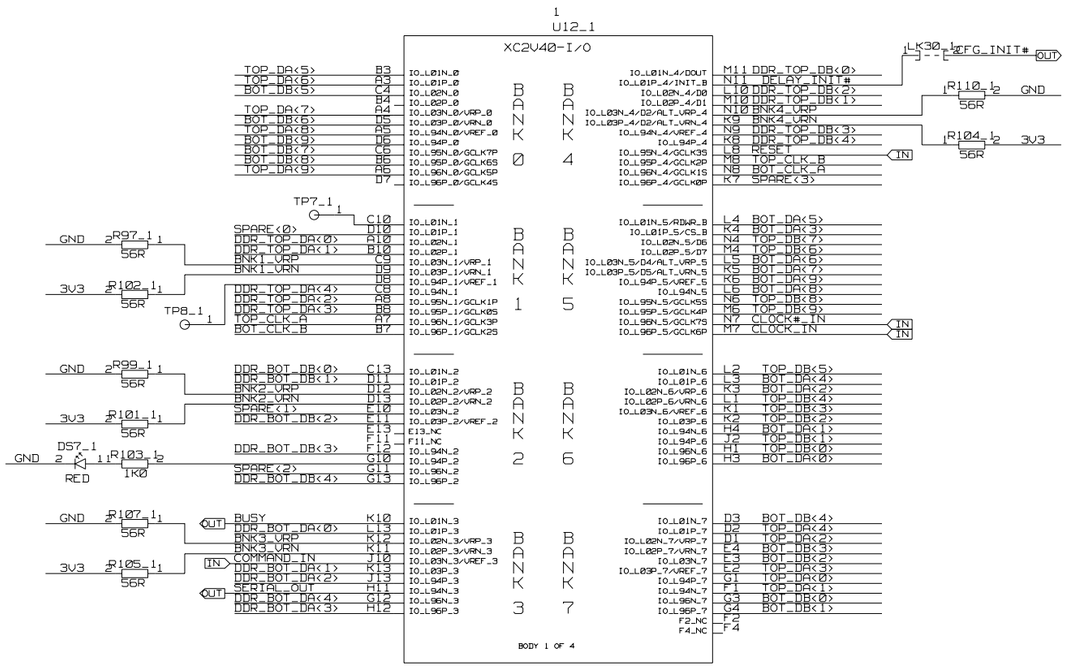

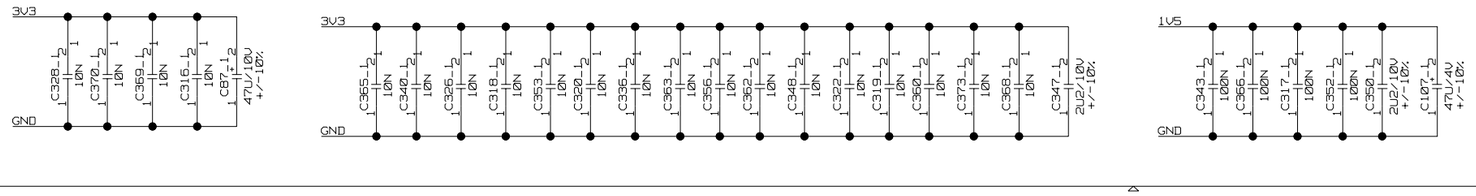

B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE

PC3205M CIRCUIT

CMS TRACKER FED
DELAY FPGA

A 2-TE-0070-020<19>B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020<19>B

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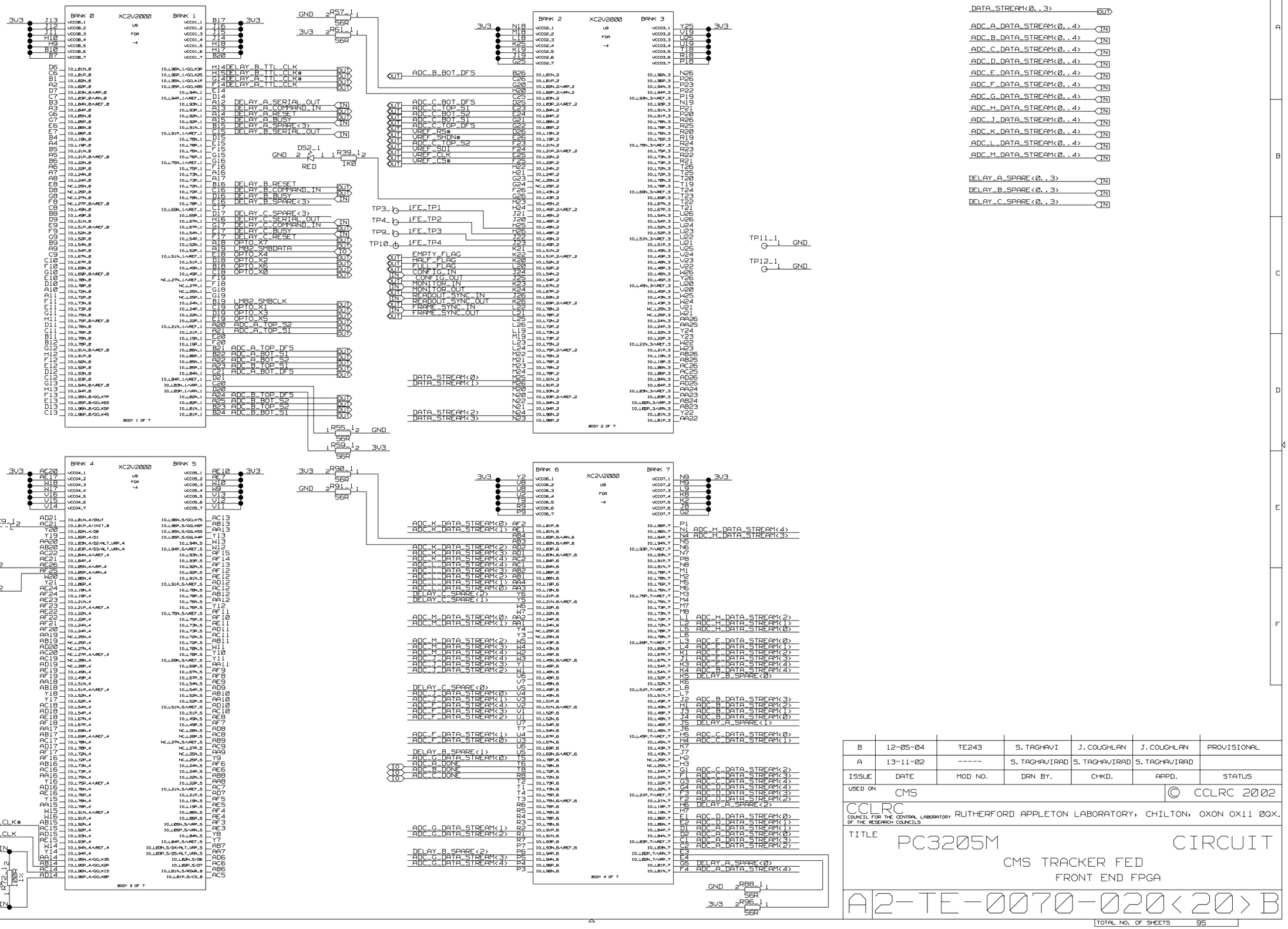

B	12-05-04	TE243	S.TAGHAVI	J.COUGHLAN	J.COUGHLAN	PROVISIONAL
A	13-11-02	-----	S.TAGHAVIRAD	S.TAGHAVIRAD	S.TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE

PC3205M CIRCUIT

CMS TRACKER FED

FRONT END FPGA

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TOTAL NO. OF SHEETS 95

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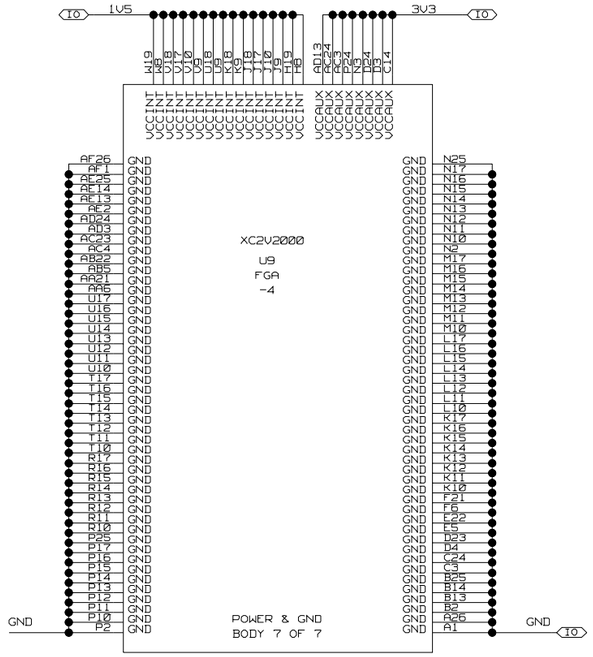

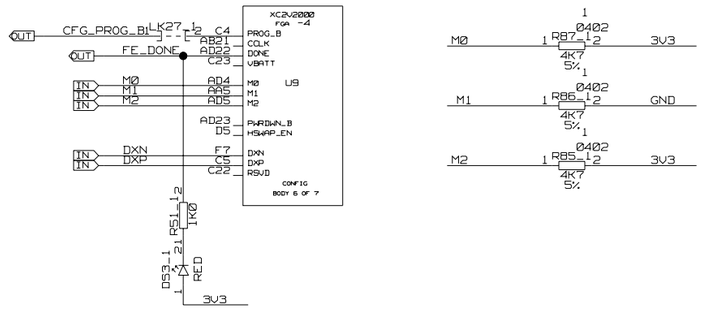

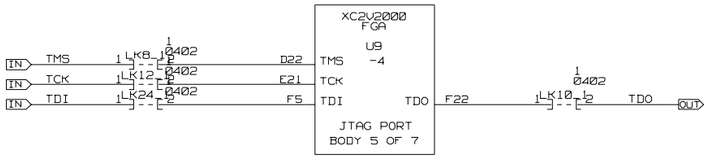

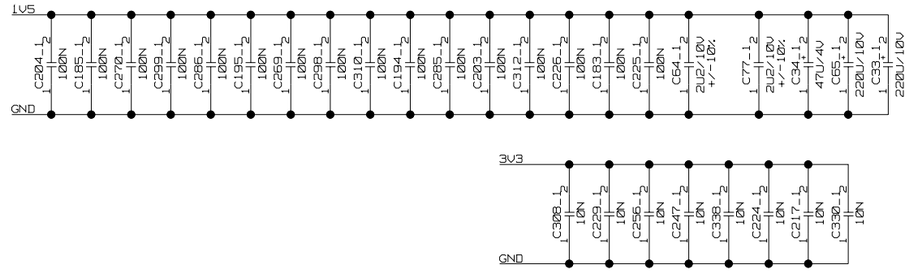

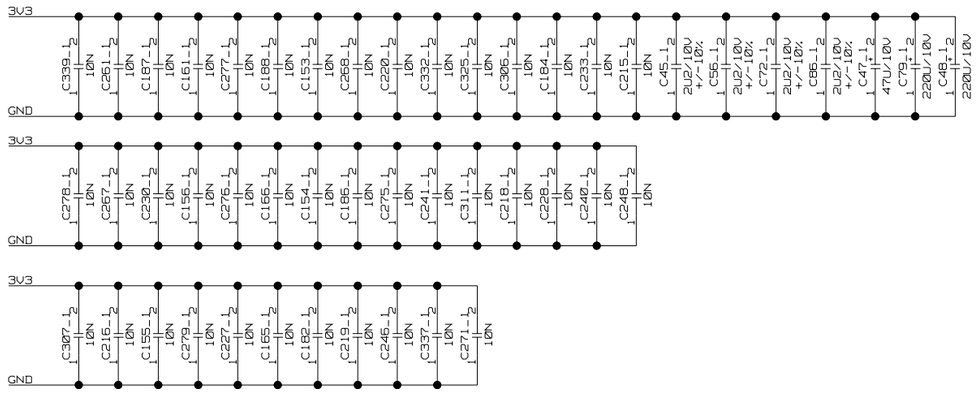

B	12-05-04	TE243	S. TAGHAVI	J. COUGHLAN	J. COUGHLAN	PROVISIONAL
A	13-11-02	-----	S. TAGHAVIRAD	S. TAGHAVIRAD	S. TAGHAVIRAD	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

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TITLE

PC3205M CIRCUIT

CMS TRACKER FED
FRONT END FPGA

A 2-TE-0070-020<21>B

TOTAL NO. OF SHEETS 95

A 2-TE-0070-020<21>B