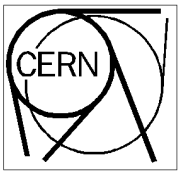

ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
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Laboratoire Européen pour la Physique des Particules
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# CMS Tracker Optical Readout Link Specification

# Part 5.1: Receiving Amplifier

**Version 4.9, 12 May 2003**

**CERN EP/CME**

EDMS DOCUMENT
CMS-TK-ES-0009

# 1. Introduction

## 1.1. General system description

This specification defines the design requirements for the analogue optical link to be used in the readout system of the tracker sub-detector of the CMS detector at the CERN Large Hadron Collider (LHC) [1.1,1.2]. The tracker sensing elements are silicon microstrip detectors. The approximate total number of detector channels is 10 millions, to be multiplexed and read-out by approximately 40000 optical links (plus spares). A thorough description of the CMS tracker is found in [1.3].

The CMS tracker optical readout link is embedded into the data acquisition chain shown in Fig. 1.1. It starts at the electro-optic opto-hybrid interface and ends at the opto-electric receiver module interface. Specifications for the Front End Driver board (FED), MUX and APV front-end chips can be found in: [1.4] and [1.5]

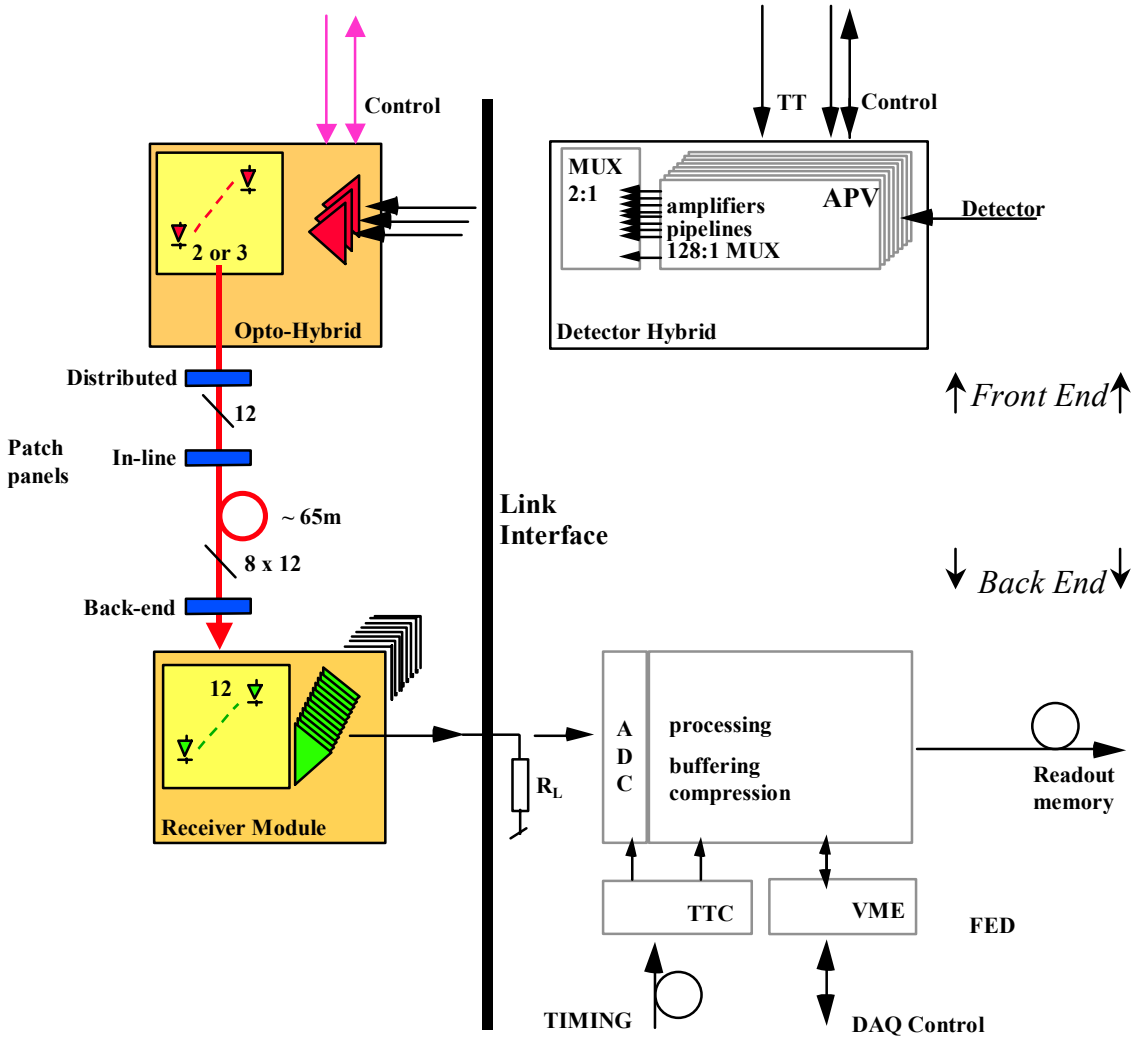


Fig. 1.1. Tracker readout chain with optical link highlighted on the left.

To ease the understanding and use of this document, a brief explanation of the CMS tracker sub-detector data flow is given below. A more detailed description of the CMS tracker readout chain can be found for instance in [1.6].
Signals from all sensor channels are sampled and stored every 25ns in the APV front-end chip analogue memory. In the event of a Level 1 trigger occurrence (TT), the analogue samples corresponding to the time slice of interest in the memory are processed, time multiplexed and transferred in packet form from the detector hybrids to the opto-hybrids via short lengths of copper (0 to 30 cm typ.). They are then sent via optical fibres to the receivers situated at the link back-end, where they are converted back to electrical. A to D conversion, processing and buffering take place on the Front End Driver (FED) boards before the data packets are sent out to the readout memory and computer farms.

## 1.2. Document structure and convention

The optical link specification is broken down into eight independent parts, each describing and specifying a different level or function in the system:

Part 1. System

Part 2. Analogue Opto-Hybrid
- 2.1 Laser Driver
- 2.2 Laser Transmitter
  - 2.2.1 Terminated Pigtail
    - 2.2.1.1 Buffered Fibre
- 2.3 Analogue Opto-Hybrid Substrate

Part 3. Terminated Fibre Ribbon
- 3.1 Ruggedized Ribbon harness
  - 3.1.1 Ruggedized Ribbon

Part 4. Terminated Multi-Ribbon Cable
- 4.1 Dense Multi-Ribbon Cable

Part 5. Analogue Opto-Receiver Module
- 5.1 Analogue Receiving Amplifier

Part 6. Distributed Patch Panel
- 6.1 MU-SR Adaptor

Part 7. In Line Patch Panel
- 7.1 MFS Adaptor

Part 8. Backend Patch Panel

Each part has the following structure:

| | | | |
|---|---|---|---|
| 1. Introduction | 2. Technical requirement | 3. Glossary | 4. References |
| 1.1. System description | 2.1. description | | |
| 1.2. Document structure | 2.2. block diagram | | |
| 1.3. Related WWW sites | 2.3. specification | | |
| 1.4. Contact | 2.4. operating environment | | |
| 1.5. Document history | 2.5. other characteristics | | |
| | 2.6. testing | | |
| | 2.7. implementation | | |

**Still to be determined parameters are labelled TBD.**

## 1.3. Related WWW sites

- CERN laboratory: http://www.cern.ch/Public/
- CMS project: http://cmsinfo.cern.ch/Welcome.html
- CMS Tracker Technical Design Report: http://cmsdoc.cern.ch/ftp/TDR/TRACKER/tracker.html
- CMS Tracker Electronic System: http://cmstrackercontrol.web.cern.ch/CMSTrackerControl/docmain.htm
- CMS Tracker Optical Links: http://cms-tk-opto.web.cern.ch/
- FED developments: http://www.te.rl.ac.uk/esdg/cms_fed_pmc/index.html
- APV and MUX developments: http://www.te.rl.ac.uk/med/

## 1.4. Contact

All questions regarding this document should be addressed to:

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## 1.5. Document history

| | |
|---|---|
| Rev. 4.1, 05/04/01 | Single ended output, 5V design, according to fast track plan |
| Rev. 4.2, 22/05/01 | TBD added to specs 5.1.21 and 5.1.29. Note added to test requirement 5.1.10. |
| Rev. 4.3, 13-14/09/01 | Specs 5.1.2, 5.1.10, 5.1.22, 5.1.26, 5.1.30, 5.1.33, 5.1.62 modified, sections 2.5 and 2.6 modified, introduction and glossary modified |
| Rev. 4.4, 19/10/01 | Figures 1.1, 1.2 modified, Specs 5.1.2, 5.1.21-5.1.28, 5.1.30, 5.1.33 modified, section 2.5 modified, glossary modified (INL). |
| Rev. 4.5, 01/11/01 | Document in conformity with Helix 9003 design, specs 5.1.3, 5.1.25, 5.1.26, 5.1.28, 5.1.31 modified, section 2.7 added. |
| Rev. 4.6, 21/08/02 | Document in conformity with Helix 9004 design, specs 5.1.36, 5.1.37, 5.1.38 added, various mistakes corrected. Intro and glossary modified. |
| Rev. 4.7, 30/09/02 | Fig 1.2 updated, specs 5.1.25, 5.1.28, 5.1.29, 5.1.37, 5.1.38, 5.1.39, 5.1.40 modified, test section 2.6 updated. |
| Rev. 4.8, 12/11/02 | Specs 5.1.37 and 5.1.38 corrected (fF units), test spec 5.1.40 modified. Spec valid for delivery H2 with 3 options HXR9004A, B and C |
| Rev. 4.9, 12/05/03 | Specs 5.1.25 and 5.1.28: note added. Spec 5.1.37 modified (Ccomp frozen). Implementation focused on one option: HXR9004AA, spec valid for production delivery H3. |

# 2. Technical requirement, part 5.1: Receiving Amplifier

## 2.1. Description

The ASIC is a 12-channel current-mode amplifier array. It converts into 12 single-ended current outputs the photocurrents generated by a 12-channel pin-photodiode array (not part of this specification). It also allows common adjustment of the DC input ($X_0$ to $X_3$) and output ($X_4$, $X_5$) offset currents as well as of the pin diode matching capacitor ($C_0$ to $C_2$).

## 2.2. Block Diagram

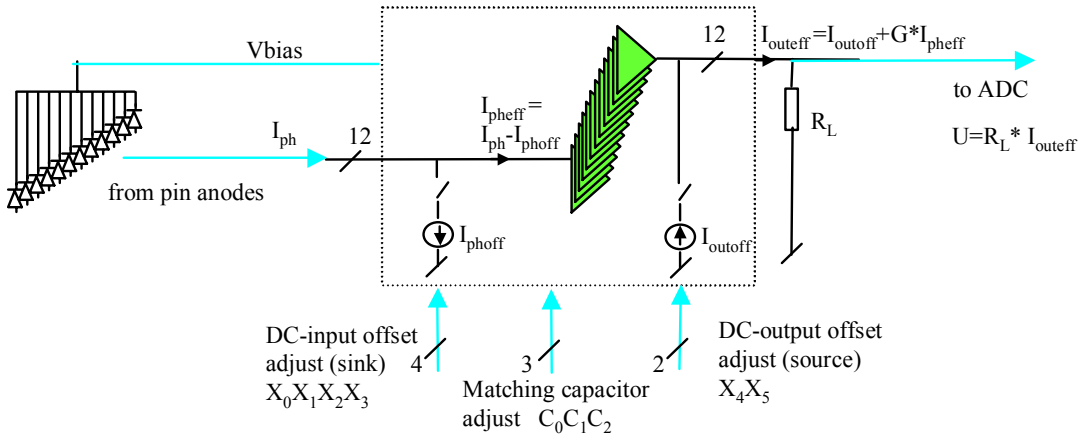



Fig. 2.1. Analogue receiver block diagram

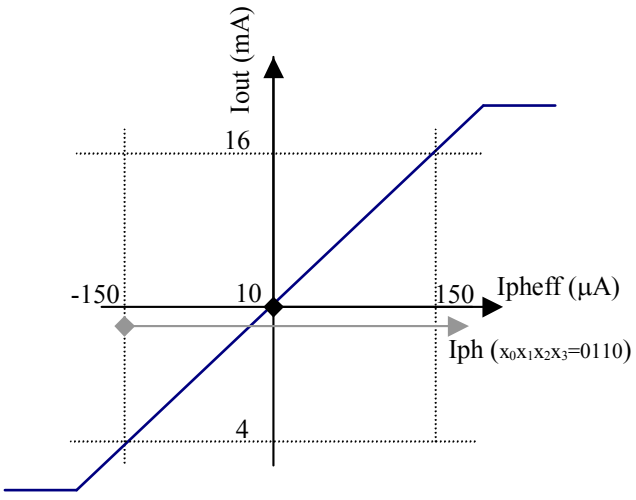



Fig. 2.2. Analogue receiver typical operating range

## 2.3. Specifications (@25°C unless otherwise noted)

| # | operational specifications | min | typ | max | unit | note |
|---|---|---|---|---|---|---|
| | | | | | | |
| 5.1.1 | Number of channels | 12 | | | | |
| 5.1.2 | Integral linearity deviation[1] | | | 1 | % | in 120μA operating input range positioned anywhere in input range. See glossary 3.1. |
| 5.1.3 | Bandwidth[1,2] | | 100 | | MHz | DC coupled, 10ns load |
| 5.1.4 | Settling time to ±1%[1,2] | | | 15 | ns | See glossary 3.2. |
| 5.1.5 | Skew | | | 1 | ns | See glossary 3.3. |
| 5.1.6 | Jitter | | | 0.5 | ns | Rms. See glossary 3.4. |
| 5.1.7 | Crosstalk[1] | | -60 | | dB | See glossary 3.5. |
| 5.1.8 | Gain **G**[1] | 38 | 40 | 42 | A/A | transimpedance $Z=GR_L$ |
| 5.1.9 | Load Resistance $\mathbf{R_L}$ | 50 | 100 | 200 | Ω | |
| 5.1.10 | Photodiode capacitance | 0.8 | 1.0 | 1.2 | pF | @ 2V reverse bias |
| | specs 5.1.11 to 5.1.20 | | | | | unused |

[1] $X_0\ X_1\ X_2\ X_3 = 0110$
[2] $C_0\ C_1\ C_2$ optimized to match photodiode capacitance

| # | electrical specifications | min | typ | max | unit | note |
|---|---|---|---|---|---|---|
| | | | | | | |
| 5.1.21 | Photocurrent input range **Iph** | | 200 | | μA | |
| 5.1.22 | Input offset current compensation **Iphoff** | 0 | | 375 | μA | User adjustable with 4bits ($X_0\ X_1\ X_2\ X_3$) Iphoff<0 means current flows into amplifier stage (see Fig. 2.1). |
| 5.1.23 | Resolution of input offset current compensation **Iphunit** | 20 | 25 | 32 | μA | Iphoff = $X_0$*Iphunit+$X_1$***2***Iphunit+ $X_2$***4***Iphunit+ $X_3$***8***Iphunit |
| 5.1.24 | Effective input current **Ipheff** | –150 | | +150 | μA | Ipheff = Iph – Iphoff Ipheff>0 means current flows into amplifier stage (see Fig. 2.1). |
| 5.1.25 | Output current **Iout** @Ipheff=+150μA | 15.4 | 16 | 16.6 | mA | Within output voltage range, assuming I(0mA)=10mA. |
| 5.1.26 | Output offset current **Ioutoff** | 0 | | 9 | mA | Within output voltage range. User adjustable with 2bits ($X_4\ X_5$) |
| 5.1.27 | Resolution of output offset current **Ioutunit** | 2 | 2.5 | 3 | mA | Ioutoff=$X_4$*Ioutunit+$X_5$***2***Ioutunit |
| 5.1.28 | Effective output current **Iouteff** @Ipheff=+150μA | 15.4 | | 25.6 | mA | Iouteff=Iout+Ioutoff, assuming I(0mA)=10mA. |
| 5.1.29 | Output voltage range | 0.4 | | 3 | V | ESD protected outputs |
| 5.1.30 | Output loading | | | 1.6 | ns | $\tau = C_L * R_L$ |
| 5.1.31 | Equivalent input noise | | | 100 | nA | Rms in 100MHz bandwidth @ Ipheff = -Iphoff = -100μA, Iph =0μA |

| | | | | | | |
|---|---|---|---|---|---|---|
| 5.1.32 | Power supply rejection ratio **ΔVcc/ΔU** | 20 | | | dB | At 1MHz, $R_L$=100Ω |
| 5.1.33 | Power supply | 4.5 | 5 | 5.5 | V | Vcc - Vee |
| 5.1.34 | Power dissipation | | | 3 | W | 12 Channels, $X_4$,$X_5$ on, to be minimized |
| | | | | 2.5 | W | 12 Channels, $X_4$,$X_5$ off, to be minimized |
| 5.1.35 | Control inputs $X_0$ $X_1$ $X_2$ $X_3$ $X_4$ $X_5$ | CMOS compatible, active high | | | | Pull downs internal to the chip |
| 5.1.36 | Control inputs $C_0$ $C_1$ $C_2$ | CMOS compatible, active high | | | | Pull ups internal to the chip |
| 5.1.37 | Compensation capacitor **Ccomp** | | 800 | | fF | |
| 5.1.38 | Resolution of compensation capacitor **Ccompunit** | 85 | 100 | 115 | fF | Selection by metal option |
| 5.1.39 | Switchable capacitor **Cs** | 0 | | 840 | fF | |
| 5.1.40 | Resolution of switchable capacitor **Csunit** | 80 | 100 | 120 | fF | Cs = $C_0$*Csunit +$C_1$***2*** Csunit + $C_2$***4*** Csunit |
| | specs 5.1.41 to 5.1.60 | | | | | unused |

## 2.4. Operating environment

| # | environmental specifications | min | typ | max | unit | note |
|---|---|---|---|---|---|---|
| 5.1.61 | Storage temperature | -20 | | 70 | °C | |
| 5.1.62 | Operating junction temperature | +20 | | 100 | °C | |
| 5.1.63 | Operating humidity | | | 60 % | RH | 13 °C dew point |
| | Specs 5.1.64 to 5.1.80 | | | | | unused |

## 2.5. Other Characteristics

- electrical interface

Wire-bonded connections inside receiver module.
External 50 to 200 Ω termination resistors on output lines.

- package

bare die

- Test Documentation and traceability:

Conformance certificate from wafer fab, test certificate from test house and description of test programme.

- Shipping and storage requirements:

Known good chips to be diced and shipped in waffle packs.

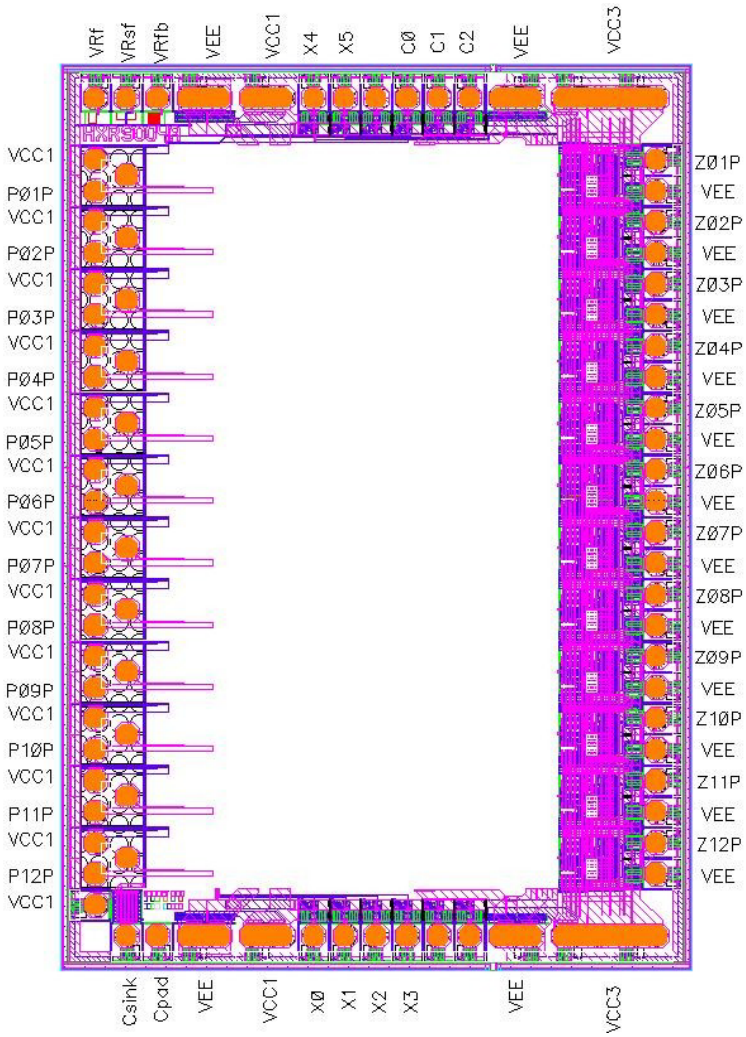
## 2.6. Testing

Chip shall be tested according to the following table:

| # | Specification to be tested | Chip Qualification in module | Chip on wafer test |
|---|---|---|---|
| | | Designer and/or CERN | Test house |
| | | | |
| 5.1.1 | Number of channels | ♦ | ♦ |
| 5.1.2 | Integral linearity deviation | ♦ | |
| 5.1.3 | Bandwidth | ♦[1] | |
| 5.1.4 | Settling time to ±1% | | |
| 5.1.5 | Skew | ♦ | |
| 5.1.6 | Jitter | ♦ | |
| 5.1.7 | Crosstalk | ♦ | |
| 5.1.8 | Gain **G** | ♦[2] | ♦[3] |
| 5.1.9 | Load Resistance $\mathbf{R_L}$ | ♦ | |
| 5.1.10 | Photodiode capacitance | ([4]) | |
| 5.1.21 | Photocurrent input range **Iph** | ♦[2] | |
| 5.1.22 | Input offset current compensation **Iphoff** | ♦[2] | ♦[3] |
| 5.1.23 | Resolution of input offset current compensation, **Iphunit** | ♦[2] | ♦[3] |
| 5.1.24 | Effective input current **Ipheff** | ♦[2] | |
| 5.1.25 | Output current range **Iout** | ♦ | |
| 5.1.26 | Output offset current **Ioutoff** | ♦ | ♦ |
| 5.1.27 | Resolution of output offset current **Ioutunit** | ♦ | ♦ |
| 5.1.28 | Effective output current **Iouteff** | ♦ | |
| 5.1.29 | Output voltage range | ♦ | ♦ |
| 5.1.30 | Output loading | ♦ | |
| 5.1.31 | Equivalent input noise | ♦ | |
| 5.1.32 | Power supply rejection ratio **ΔVcc/ΔU** | ♦ | |
| 5.1.33 | Power supply | ♦ | |
| 5.1.34 | Power dissipation | ♦ | ♦ |
| 5.1.35 | Control inputs $X_0$ $X_1$ $X_2$ $X_3$ $X_4$ $X_5$ | ♦ | ♦ |
| 5.1.36 | Control inputs $C_0$ $C_1$ $C_2$ | ♦ | ♦ |
| 5.1.37 | Compensation capacitor **Ccomp** | | |
| 5.1.38 | Resolution of compensation capacitor **Ccompunit** | | |
| 5.1.39 | Switchable capacitor **Cs** | ♦ | |
| 5.1.40 | Resolution of switchable capacitor **Csunit** | ♦ | |
| 5.1.61 | Storage temperature | | |
| 5.1.62 | Operating junction temperature | ♦ | |
| 5.1.63 | Operating humidity | | |
| | Channel to channel uniformity | ♦ | ♦ |

([1]) Measured as rise-time.
([2]) Measurement is convoluted with pin response.
([3]) Gain and Iphoff measurements during automated testing are convoluted.
([4]) Photodiode capacitance will be directly measured on the receiver modules.

## 2.7. Implementation: HXR9004AA




AMS 0.8µm BiCMOS process, all pad centers on 125 µm grid.

| Dimensions: | X (µm) | Y (µm) |
|---|---|---|
| Thickness: | 535 µm ± 25 µm | |
| Design size | 2525 | 3650 |
| Scribe line width | +100 | +165 |
| Repeat distance | 2625 | 3815 |
| Saw cut loss | - 50 | - 50 |
| approx. die size | 2575 | 3765 |

# 3. Glossary

## 3.1. Integral Non-Linearity

The integral non-linearity INL is defined as the operating-range-normalized error one makes when, for a given link output signal y, the link input signal is assumed to be the linearized value $x_L$ instead of the real value x.

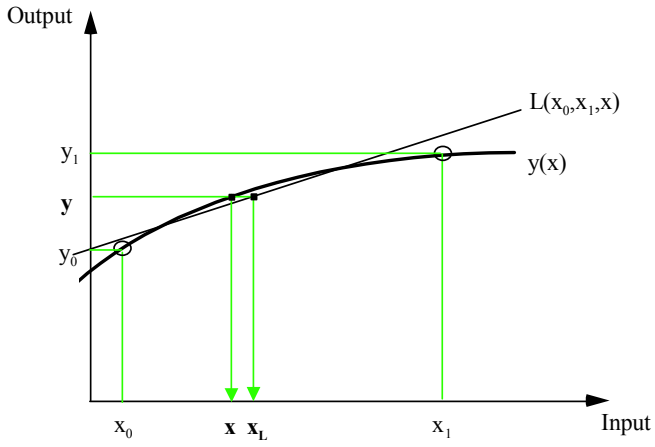



Fig. 3.2. Integral non-linearity

The linear regression is calculated by fitting the transfer characteristic in the linear range $]x_0, x_1]$ (alternatively $]y_0, y_1]$ in the output range) .

INL is defined as the error one makes when approximating x by $x_L$, normalised by the operating range $x_1 - x_0$:

$$INL = \frac{x - x_L}{x_1 - x_0}$$

The operating range can be anywhere within the full input range.

## 3.2. Settling time

The settling time is defined as the time required for a step response signal to settle to ±1% of its end value.

## 3.3. Skew

The skew is determined by measuring, for two channels, the average time $\overline{t_{50}}$ required for a step response signal to reach 50% of its end value. The skew between channels i and j is defined as:

$$t_{skew} = \overline{t_{50,\,j}} - \overline{t_{50,i}}$$

### 3.4. Jitter

The rms jitter is defined as the rms deviation of the time $t_{50}$ required for a step response signal to reach 50% of its end value:

$$t_{jitter} = \sqrt{\overline{(t_{50} - \overline{t_{50}})^2}}$$

### 3.5. Crosstalk

The crosstalk between two channels i and j is defined as the relative feedthrough from channel i to channel j at sampling time $t_s$=20ns when an ideal step signal is injected into channel i at t=0s.

$$\text{Crosstalk} = 20\,\text{Log}\left|\frac{Out_j}{Out_i}\right|_{t_s=20\,ns}$$

## 4. References


[1.1] http://cmsinfo.cern.ch/Welcome.html/

[1.2] http://www.cern.ch/, or http://public.web.cern.ch/Public/

[1.3] The tracker project, technical design report, CERN/LHCC 98-6, CMS TDR 5, http://cmsdoc.cern.ch/ftp/TDR/TRACKER/tracker.html http://edms02.cern.ch/tmpfiles/edms_tmp_1708833_addendum.pdf

[1.4] R. Halsall, "FED specifications", Draft, RAL, http://www.te.rl.ac.uk/esdg/cms-fed/

[1.5] APV 25 User guide, RAL http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/CMS/APV25-S1/pdf/User_Guide_2.2.pdf MUX User guide, RAL http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/CMS/APVMUXPLL/pdf/UserGuide.pdf

[1.6] G. Hall, “Analogue optical data transfer for the CMS tracker”, Nuclear Instruments and Methods in Physics Research A, Vol. 386, pp. 138-42, 1997.

[1.7] A. Marchioro, " Specifications for the Control Electronics of the CMS Inner Tracker", Draft V2, CERN, http://cmstrackercontrol.web.cern.ch/CMSTrackerControl/documents/RocSpecsV2.pdf

[1.8] A. Marchioro, "FEC specification", Draft, CERN

[1.9] A. Marchioro, "CCU specification", Draft, CERN, http://cmstrackercontrol.web.cern.ch/CMSTrackerControl/documents/Sandro/Ccu260598.pdf

[2.1] M. Huhtinen, “Studies of neutron moderator configurations around the CMS inner tracker and Ecal”, CERN CMS TN/96-057, 1996.

[2.2] http://www.cern.ch/CERN/Divisions/TIS/safdoc/instr_en.html