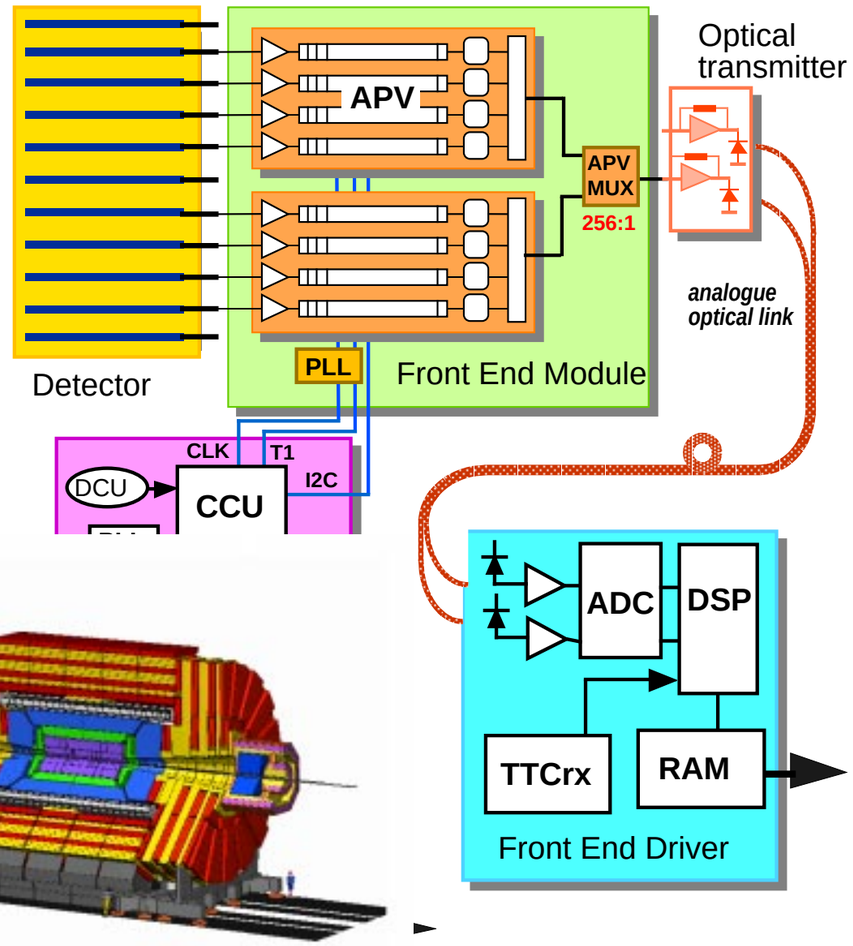
http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

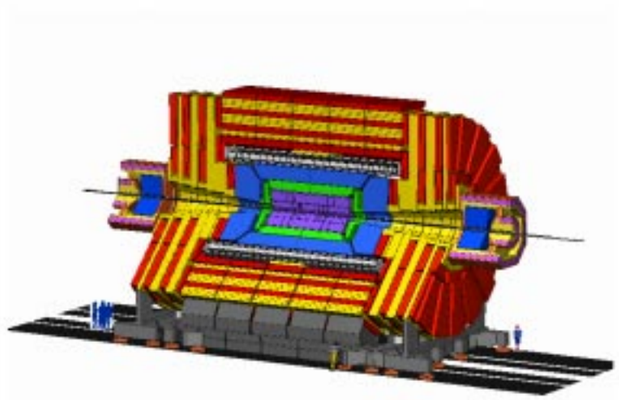
A PMC Based ADC Card for CMS Tracker Readout

S.A. Baird, P. Burch, J.A. Coughlan, R. Halsall
J. Hartley, W.J. Haynes, T. Parthipan, T. Slade

CLRC Rutherford Appleton Laboratory
Chilton, Didcot, Oxon OX11 0QX
United Kingdom

CMS Microstrip Tracker Readout





Microstrip Tracker : Silicon & MSGCs

Total => 12,000,000 readout channels

≈70% CMS final data volume

LHC Clock @ 40 MHz

CMS Level 1 Trigger @ ≈ 100 kHz

Analogue Readout

Front End Pipelines APV on Detector

Front End Drivers FED in Counting Room

Each FED ADC Channel reads out 256 Microstrips

FED Functions:

- Optical Receivers
- ADCs
- Digital Signal Processing
- Error Detection
- CMS Central DAQ Interface

CMS Detector at LHC starts up in 2005

http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

CLRC

FED-PMC

...see one here Today!

http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

Requirements:

- **Tracker Detector Prototyping**
- **Evaluating Final FED Components**

Solution:

PCI Mezzanine Card PMC format

Compact, Modular
Commercial Bus PCI
Plug on "off the shelf" VME Carriers
Plug in PC/Workstation

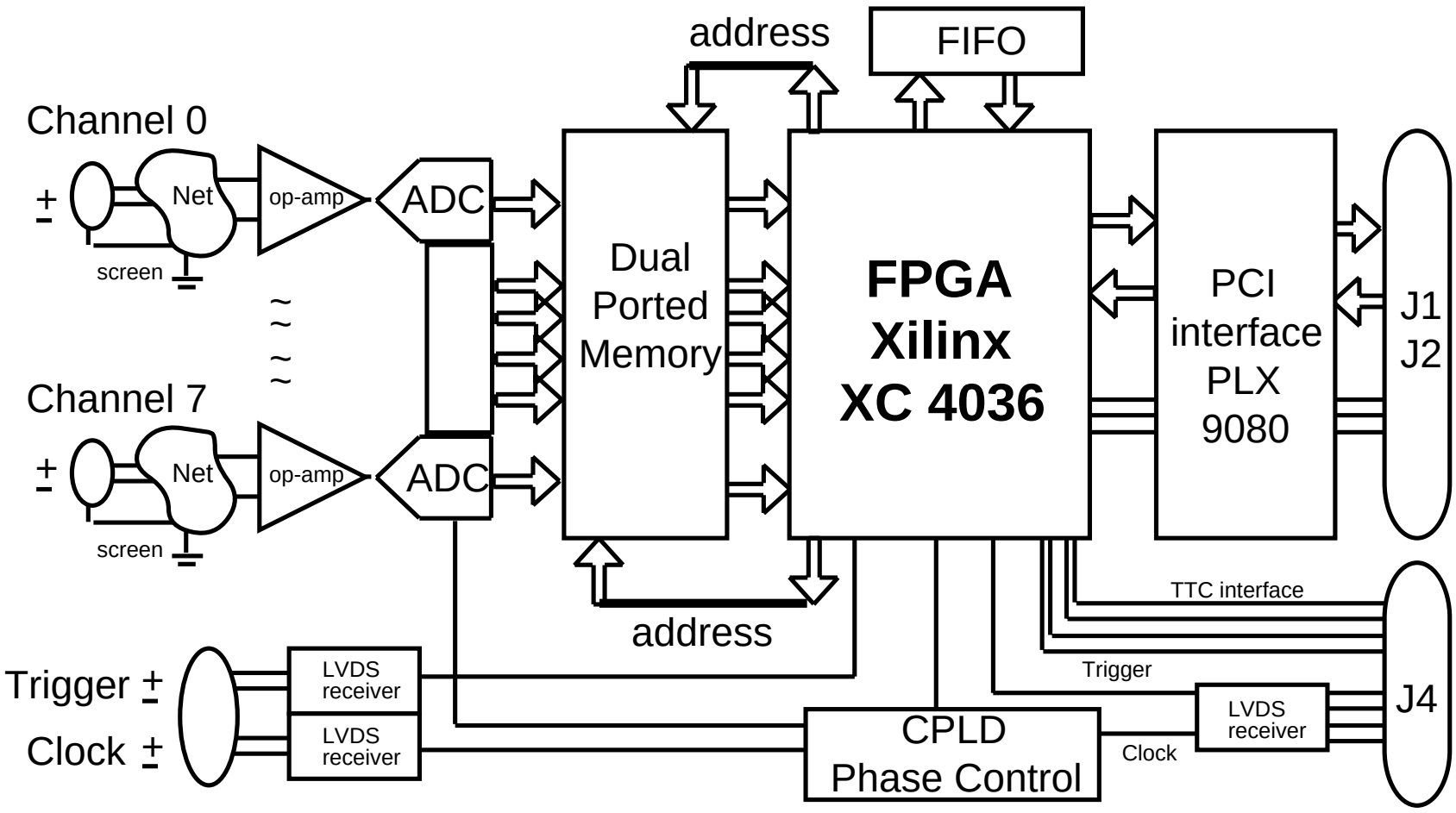
Providing a Flexible & Cost Effective Solution for Test Beam and Lab setups

Standards:

Hardware : PMC
Firmware : VHDL
Software : C Drivers

Designed at RAL CLRC

Functionality



8 Electrical Input Channels (Differential/Single-ended)

Clock & Trigger LVDS via Front Panel (or Rear Connector)

ADCs commercial 9 bit @ 2 to 40 MHz

Data Buffer in DPM => 64K samples/channel

Parallel Readout via

PCI Interface 32 bit @ 33 MHz

FPGA with VHDL for *Flexible Architecture*

Plus...

- **Test Functions**
- **Clock Phase Adjustment**
- **FPGA Flash Memory**
- **FIFO**

http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

CLRC

Firmware & Software

Firmware & Software Integrated Package

Firmware *FPGA*

Core VHDL Blocks

Local Bus
DPM Interface
Buffer Management
FIFO & Counters control
Register Interface
Test Functions

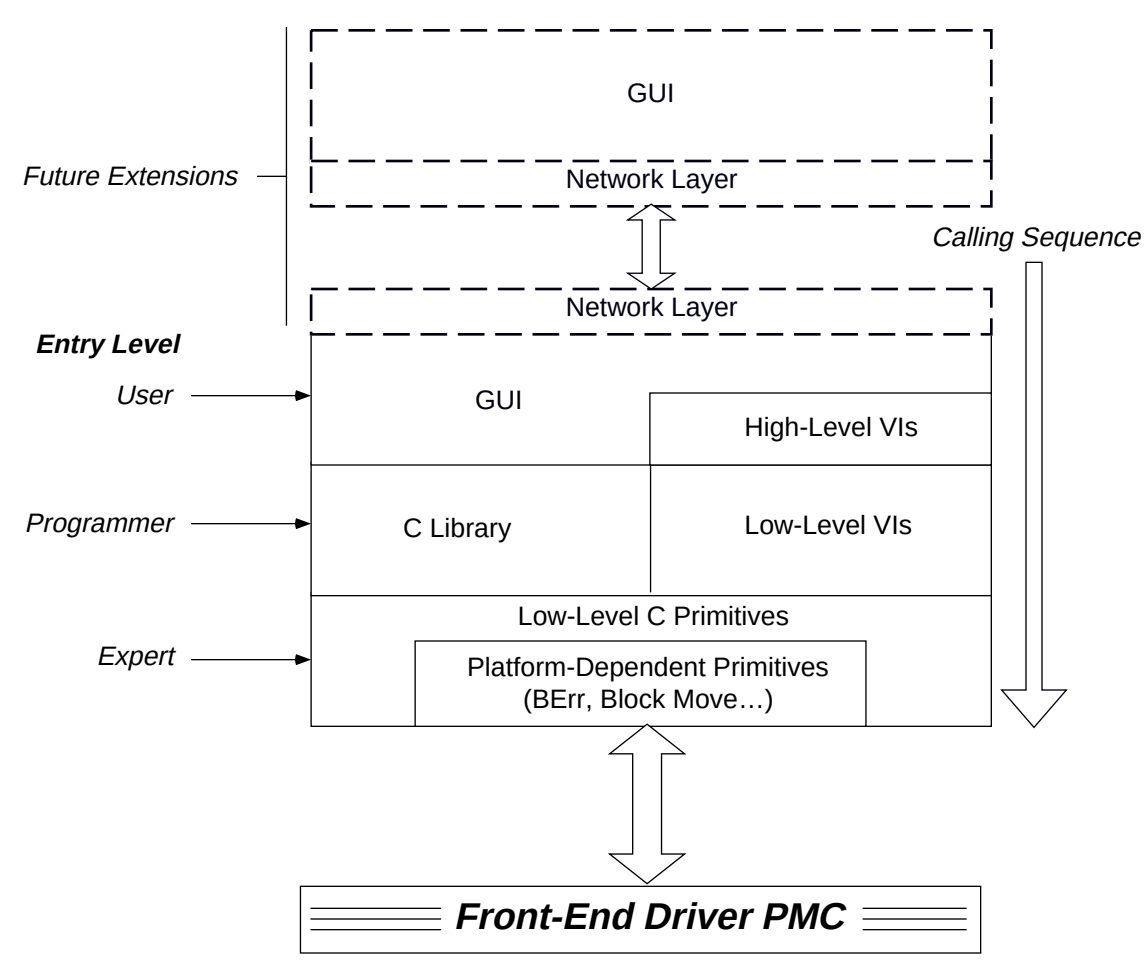
Future Extensions

APV Auto-Synchronisation
Higher Level DAQ Interface
Hit Finding

Firmware can be updated *in situ* via Network

Open Firmware Architecture complemented by...

Software *Layered Design*



End User Advantages

Hide Hardware Details
Minimise code effort
Manage Firmware updates

Running with

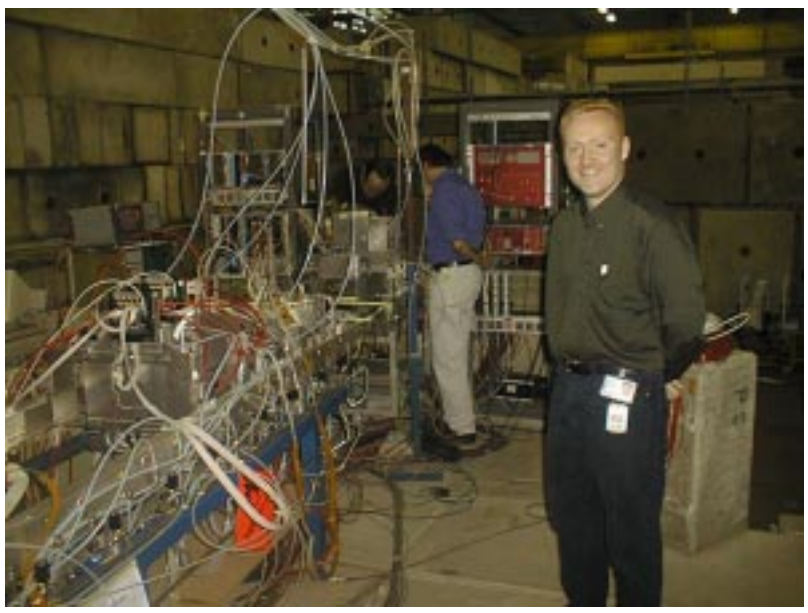
LynxOS, VxWorks

http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

CLRC

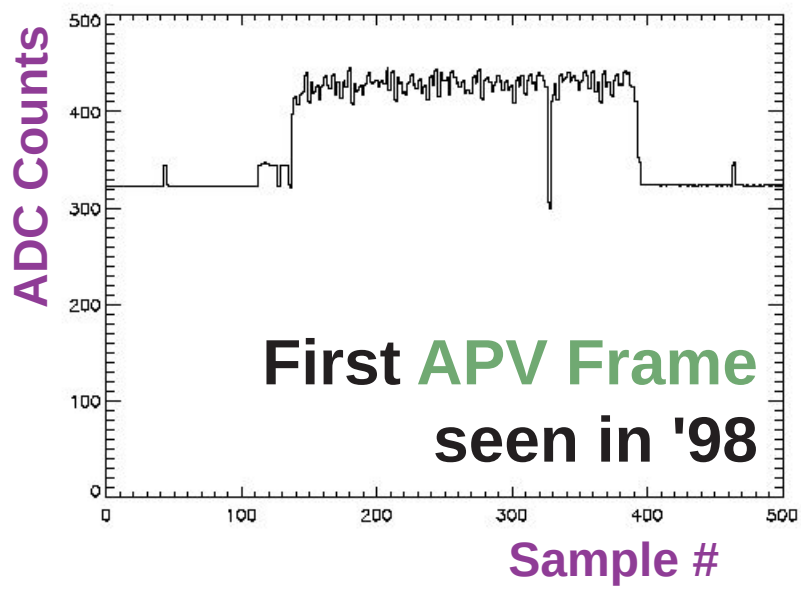
Status

FED-PMC **Mk1** commissioned at **CERN** Test Beam **Oct'98**



FED-PMC **Mk2** used by all Detectors at **CERN** Test Beam **May'99**

20 Mk2 FED-PMC's produced in **1999** for **CMS** Tracker Community



First APV Frame seen in '98

Future

Next **Milestone** at **25 nsec** Test Beam **CERN 2000**

- APV Synchronisation
- Central DAQ Interface

Applications *outside* CMS...

- *LHCb*
- Medical Imaging
- General Purpose ADC Card
- +...???

http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

CLRC