Contribution of FED header to Data Rate

- Existing data rate study (CMS Note 2002/047):
  - FRL merges data from 1-2 FEDs (now 1-4 ?) and has output bandwidth = 200 MB/s.
  - Assume 112 Byte FED header, so at 100 KHz & 2 FEDs/FRL, get 2*10.7 = 21.4 MB/s/FRL.

- Greg notes:
  - Current FED header **848 Bytes !**
    - 8 FE-FPGA headers each 16 bytes = 128 Bytes
    - 96 Fibre headers each 7 bytes = 672 Bytes
    - S-link padding ? = 32 Bytes

- John, Ian, Said or Greg suggest:
  - Fibre header: remove "packet code" (FED mode) and 2*CM (saves 5*96 Bytes).
    replace "fibre (data) length" by number clusters (saves 96 Bytes).
  - FE-FPGA header: remove "zeros" (8*4 Bytes). drop data length (8*2 Bytes) ?
    - "Frame sync packet": compress APV error flags (96*6 bits→96*(2-4) bits) ?
      drop majority pipeline addr. (8*1 byte) ?
    - "BE status reg.": drop FIFO fullness (3 Bytes) ?

- **If do everything, get FED header of: 848 – 576 – 48 – 56 – 3 = 176 Bytes.**